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The Next Silicon Decade: Designing a Resilient Semiconductor Ecosystem for Europe

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Executive Summary

Europe's grand strategy for semiconductor sovereignty has finally collided with reality. For years, Brussels and major EU capitals tried to buy their way into the global chip race by simply mimicking the U.S. and Taiwan, throwing massive subsidies at giant, single-site factories. But this copy-paste approach ignored three hard truths about the European market: (i) the absence of a domestic hyperscaler demand base capable of absorbing leading-edge logic at scale, (ii) the cost and volatility profile of European energy and permitting, and (iii) the fragility of sovereignty-by-FDI when the real power variables remain on a foreign corporate balance sheet.

The cancellation of Intel's Magdeburg mega-fab plan and Intel's planned Poland packaging plant shows how quickly headline commitments can reverse with corporate capital cycles. This setback removes one project but it exposes the strategic flaw of a cathedral in the desert approach where European resilience is tied to a small number of isolated mega-bets.

The appropriate response is to adopt a doctrine of defensible ecosystems grounded in Europe's structural conditions. A defensible ecosystem is one that continues to function and confer strategic leverage under conditions of supply chain coercion, export controls, sabotage, and acute disruption. These scenarios include conditions where access to Taiwan-class leading-edge compute is partially or temporarily disrupted. At the same time, the ecosystem positions Europe to shape the "next generation" of architecture beyond monolithic Moore's-Law scaling. The next decade's competitive terrain will be defined as much by advanced packaging, chiplets, 3D integration, silicon photonics, wide-bandgap power electronics, and security-anchored lifecycle assurance as by raw transistor density.

This brief therefore proposes a shift from treating fab capacity as the definition of sovereignty to treating it as a supporting asset inside a broader an architecture of resilience and leverage. Europe should still build and retain credible capacity, but sovereignty is won when that capacity is embedded in the nodes and layers that are (a) economically viable on European soil, (b) strategically sticky because they are hard to relocate, (c) politically distributable across member states, and (d) decisive for the operation of European automotive, industrial, energy, and defense systems. The recommended model is a pan-European hub-and-spoke ecosystem built upon five pillars:

- **Utility-Node Anchors which secure the "industrial workhorse" nodes (12nm-90nm) that keep the €4 Trillion European manufacturing base running.**
- **A federated network of advanced packaging and test facilities that captures value at the "chip-to-system" joint.**
- **The Rapid Prototyping Frontier Foundry (RPFF): A new mechanism to maintain competence in <5nm AI design and auditing without engaging in a futile volume-subsidy race at the leading edge.**
- **A "European Assurance" regime and an "Atlantic Shield," operating together as a powerful demand-creation engine. This framework uses European market access as a diplomatic lever to force reciprocity from others, while funding domestic resilience at home.**
- **Ecosystem equity and infrastructure: require enabling infrastructure alongside industrial subsidies and align worker incentives through structured participation.**

A second correction is required. The global semiconductor world is now bifurcating, but not cleanly. A legacy sphere is being pressured by overcapacity and price tactics; an advanced sphere is being weaponized by export controls and geopolitical risk. Europe is squeezed between the two. The solution is not to pick one sphere and imitate it; it is to become indispensable at the joints between spheres: packaging, validation, photonic interconnect, power modules, certified provenance, and upstream materials processing. In a fragmented world, the most durable resilience is not self-sufficiency; it is enforced relevance at chokepoints.

1. A Baseline Check of Where Europe Stands in 2026

Any European semiconductor strategy must support the Union's strategic objectives. And it must be grounded in a clear 2026 baseline rather than in aspirational targets. Three facts now define the current landscape.

First, the "single-site mega-fab as flagship sovereignty" model has proven fragile. Intel's cancellation of Magdeburg and its packaging plan in Poland was not a minor delay; it confirmed that projects premised on one foreign firm's capital allocation are exposed to cyclical demand, internal restructuring, and cross-Atlantic strategic reprioritization. Europe can and should remain open to FDI, but it cannot architect its industrial security around it.

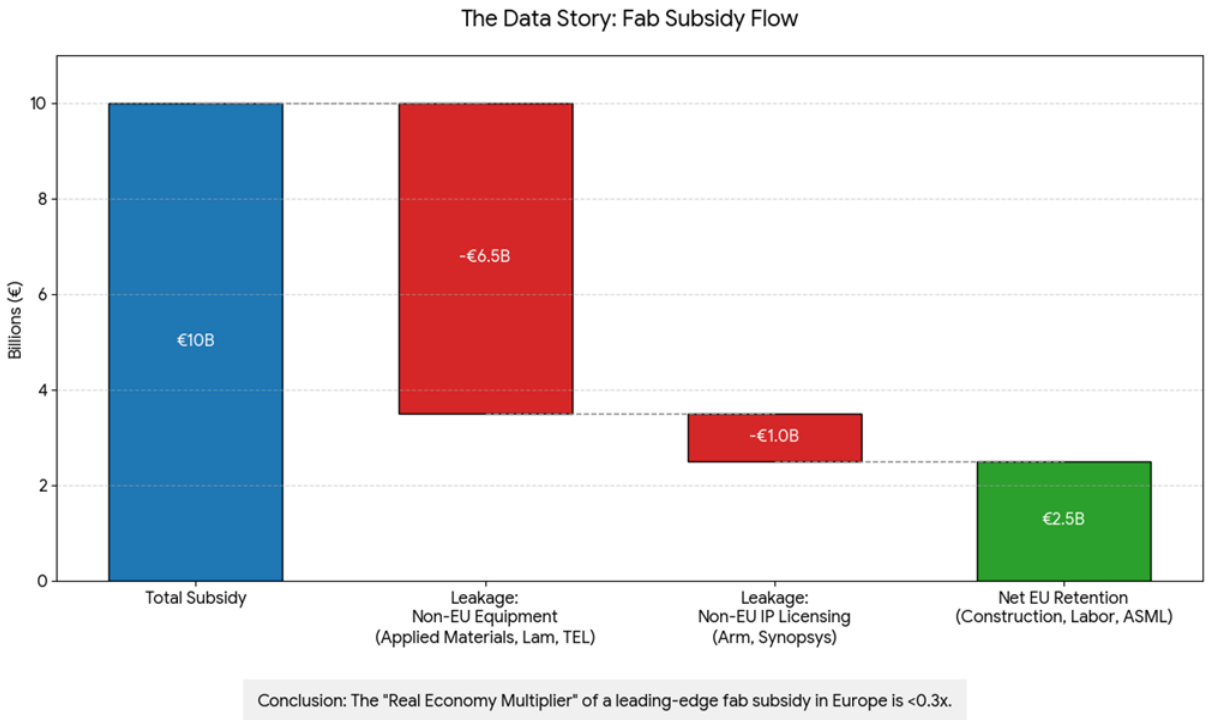
Further, the "Mega-Fab" model (e.g., Magdeburg) requires massive CAPEX for capacity that exceeds European demand, with high subsidy leakage to non-EU equipment vendors. The solution is a distributed Advanced Packaging Network providing higher job creation, better alignment with EU industrial needs, and redundancy for a fraction of the subsidy cost. The analysis in the table below answers the question "What if we took the subsidy intended for one Intel Magdeburg and spent it on facilities like the one in Poland?"

Figure 1.1: Comparative Return on Sovereignty (RoS) (illustrative scenarios)

Metric	Scenario A: Single Mega-Fab (Ref: Intel Magdeburg)	Scenario B: Packaging & Test Grid (Ref: 3x Sites like Intel Poland/Amkor)	Delta (Efficiency)
Total Project CAPEX	€30.0 Billion	€13.8 Billion (3 x €4.6B)	54% Lower Cost
Public Subsidy Required	€10.0 Billion (33% intensity)	€4.0 Billion (29% intensity)	€6.0B Savings
Direct Job Creation	~3,000 Jobs	~6,000 Jobs (3 x 2,000)	2x Jobs
Subsidy Cost Per Job	€3.33 Million / Job	€0.67 Million / Job	5x More Efficient
Time to first output (wafer/unit)	48–60 Months	18–24 Months	2.5x Faster
Sovereignty Outcome	1 Single Point of Failure	3 Redundant Nodes (Hub-and-Spoke)	Resilient Network
Primary Beneficiary	US Equipment Vendors (AMAT/Lam/KLA)	EU Auto/Ind. Integrators (BMW, Siemens)	Local Value Capture

As the table above illustrates, for 40% of the subsidy cost of one Mega-Fab, Europe could build double the employment capacity across three different member states. It also shows that Scenario A suffers from "Sovereignty Leakage." Approximately 60-70% of the CAPEX in a leading-edge fab is spent on equipment. While ASML (EU) captures lithography, deposition/etch/metrology tools are largely supplied by US and Japanese firms. Thus, €6-7B of the €10B subsidy effectively leaves the EU immediately to purchase foreign tools. Backend facilities have a higher ratio of construction/infrastructure to equipment, retaining more stimulus within the EU construction and labor sectors.

Figure 1.2



Source: author calculations

Second, Europe's most credible near-term manufacturing anchor is not the angstrom frontier; it is the utility-node and advanced-mature range serving automotive and industrial demand. The TSMC-led ESMC Dresden project is explicitly scoped for 28/22nm planar CMOS and 16/12nm FinFET, with a targeted production start in 2027 and a planned capacity of 40,000 300mm wafers per month. That node range maps directly to the microcontrollers, connectivity, and safety-critical logic that underpin the European car, factory, and grid.

This scope is supported by the "GDP-at-Risk" Index. Data indicates that 85% of Europe's industrial value-add (comprising automotive, industrial IoT, and aerospace sectors) depends primarily on >12nm nodes. In stark contrast, the <7nm market serves a hyperscale consumption base that Europe currently lacks. This represents <5% of domestic wafer demand. Consequently, a strategy myopically focused on sub-2nm fabrication addresses a market that does not yet exist in Europe, while leaving the continent's actual economic engine exposed to supply shocks in the legacy nodes it cannot function without.

Figure 1.3: The European GDP-at-Risk Index (2026 Projections)

Industrial Sector	Est. Share of EU GDP	Critical Node Dependency	Primary Use Cases	Supply Vulnerability
Automotive & Mobility	**~7%** (Direct)	**28nm – 90nm+**	MCUs, Power Electronics (SiC/ GaN), Inverters, ADAS Sensors	**Critical.** Global legacy capacity is shrinking as fabs convert to finer nodes, yet demand here is tripling.
Industrial IoT & Engineering	**~14%** (Manufacturing)	**40nm – 180nm**	Analog sensors, Actuators, Power Management ICs (PMIC), Robotics	**High.** Relies on "depreciated assets" (old fabs that are prone to breakage and lack investment.)
Aerospace & Defense	**~2%**	**65nm – 350nm**	Radiation-hardened logic, RF communications, legacy avionics	**Severe.** Security of supply is paramount; these chips must be made on trusted soil, not imported.
Hyperscale / AI Compute	**<1%** (Domestic Hardware)	**<5nm – 2nm**	GPU training clusters, High-Per- formance Computing (HPC)	**Low (Domestic).** Europe consumes these services but manufactures negligible hardware in this class.

(Analysis of semiconductor dependency by industrial sector versus node size.)

Source: Author Analysis based on data from VDA (Verband der Automobilindustrie), McKinsey, Deloitte, Kearney, Interface, Eurostat

Figure 1.3 shows why the utility-node pivot is more about protecting the existing economic base rather than a pure technology play. The reader can see that this reveals that a supply chain rupture in the 40nm-90nm range would paralyze approximately 23% of Europe's GDP (Automotive + Industrial Manufacturing). A similar rupture in <2nm would impact less than 1% of direct domestic production value.

Third, the 20% global market-share target for 2030 is now widely assessed as unlikely under current funding and implementation conditions. The European Court of Auditors has explicitly stated it is unlikely the EU will meet the 20% objective. This matters because an unattainable KPI tends to warp policy toward symbolic actions and away from defensible ones. The policy objective must shift from global volume share to operational survivability, assured supply for critical sectors, and strategic leverage in chokepoints.

Lastly, the recent "Greenland Factor" has redefined Supply Risk. Previous models assumed a binary world: "Safe" (US/EU/allies) vs. "Risky" (China). The ongoing Greenland Rift which is characterized by the tensions surrounding Transatlantic trade negotiations and the US threatening tariffs on EU high-tech exports has invalidated this. We must now model a "Tri-Polar Risk" environment where access to US technology stacks (IP, EDA tools, and frontier silicon) could be leveraged as a coercive tool against Brussels.

This baseline also clarifies political direction. A "Semicon Coalition" was launched by nine member states in March 2025 (Austria, Belgium, Finland, France, Germany, Italy, Poland, Spain, the Netherlands), and subsequently endorsed in a declaration signed by all 27 member states, calling for a revised Chips Act. The European Parliament's legislative train indicates the Commission intends to publish a Chips Act II proposal in Q1 2026.

The strategic takeaway is clear: Chips Act 2.0 must be more than just a giant subsidy fund; it needs to actively connect the entire European tech sector. The main question for Europe is no longer simply about paying to build new factories. The real test is whether it can build a resilient, interconnected industry that actually functions when global supply chains are under pressure.

Therefore, the 2026 baseline should be read as a constraint map that forces doctrine-level trade-offs: Europe can credibly anchor utility-node supply for its industrial base, but it cannot sustainably purchase frontier-node parity through subsidies alone; it can distribute resilience through backend custody and validation capacity, but it cannot gamble sovereignty on a small number of prestige sites; and it can convert regulation and procurement into stable demand, but only if governance and enforcement are explicit rather than assumed.

2. Why “defensible ecosystems” now: Europe’s squeeze and the false comfort of capacity

The global semiconductor trade is hardening into hostile blocs. The threat spans potential conflicts like a Taiwan invasion to active Middle East wars disrupting energy and critical upstream gases like Qatari helium. It also includes the routine weaponization of interdependence: export licensing, “dual-use” controls, and price tactics that destroy nascent competitors.

China’s strategic semiconductor inputs and strategic semiconductor inputs controls which were first announced in mid-2023 and then echoed by subsequent rounds of restrictions and licensing actions, illustrated a key point: Europe’s vulnerability is at the wafer but more so the materials and processing stages that can be interrupted quickly. Simultaneously, Europe’s reliance on external frontier compute is becoming increasingly consequential. In a Taiwan contingency, a disruption in access to 3nm-class compute would not merely slow consumer electronics; it could constrain European defense production, secure communications, industrial automation upgrades, and parts of energy-system modernization.

A manufacturing-centric strategy is inherently brittle. First, physical capacity is transient; it can be replicated elsewhere, canceled, or reallocated as corporate priorities shift. Second, the EU’s structural disadvantages: higher cost of energy and construction, permitting timelines, and the lack of a large domestic frontier logic customer base, cannot be fully compensated with subsidies without creating a permanent fiscal sink.

A defensible ecosystem is different and is designed to withstand these disruptions and pressures. It creates “stickiness” through integration layers that are expensive to rebuild and whose value does not vanish when one fab slips. To achieve durable competitiveness, Europe must move beyond simple subsidies and reinforce four mutually supporting conditions:

Factor conditions (build and harden): Europe must leverage cluster-grade energy reliability, chemical proximity zones, trusted backend custody capacity, and mobile human capital (European semiconductor coordination framework). These factors reduce yield risk, shorten supply chains for volatile inputs, and make high-assurance operations viable on European soil.

Demand conditions (manufacture and stabilize): A “European assurance” regime creates a predictable, high-assurance demand floor in defense and defined critical infrastructure. Simultaneously, a calibrated targeted procurement incentive prices security externalities without triggering maximal retaliation dynamics.

Related and supporting industries (turn adjacency into moat): Europe’s chemicals base, metrology and precision engineering, industrial automation, and automotive/energy system integrators become value-capture layers. They provide qualification services, validated reference architectures, and lifecycle assurance, making the ecosystem harder to unwind because it is embedded in standards and tooling.

Rivalry and market design (prevent stagnation): Chips Act 2.0 must fund capabilities, not champions. It should create regulated competition among EU nodes and operators through performance-based tenders, transparent certification tiers, and auditability so the ecosystem innovates instead of cartelizing.

The necessary change in mindset is also political. The semiconductor value chain must be distributed beyond the traditional “Blue Banana” corridor to bind the Union together. A purely Rhineland-centric strategy creates political resentment and weakens Union cohesion. A hub-and-spoke ecosystem, by contrast, creates specialized roles for peripheral and Central-Eastern member states, providing each region with a stake in the industrial future while simultaneously improving resilience by avoiding single-point failures.

3. The Next-Generation pan-European Architecture

A 2026-2035 architecture must do three things at once: protect the “workhorse” technologies needed for Europe’s industrial base today, maintain a “competence foothold” in the AI frontier without bankrupting the bloc, and seed the “next generation” of semiconductor architecture (3D integration, chiplets, photonics, and post-CMOS pathways) so Europe is shaping the frontier rather than renting it.

3.1 Anchor hubs: utility nodes with credible demand

Saxony (Dresden) and similar hubs should focus on utility nodes and advanced-mature FinFET. With ESMC, the correct objective is to secure robust European capacity at 28/22nm and 16/12nm as a defensive moat for automotive and industrial systems, precisely because these nodes map to long-lifecycle markets where qualification and reliability matter more than bleeding-edge density.

France’s Crolles/Grenoble axis remains strategically important as a specialty/R&D gravity center. The policy lesson from recent European volatility is not to abandon Crolles-type clusters, but to ensure the ecosystem does not collapse if any one site delays or resizes. Therefore, the French hub should be treated as one pillar in a redundant system, tightly coupled to packaging pilots, reference design platforms, and European PDK standardization so its value persists even through cyclical capex shifts.

This is the defensive moat for automotive and industrial systems. The goal is to secure enough capacity to sustain Europe’s critical infrastructure under disruption, including independently of Asian foundries if necessary.

3.2 Backend sovereignty as a network, not a single bet

Intel’s cancellation of the Poland integration plant forces a redesign: Europe must build backend sovereignty as a federated network across multiple sites and operators, not as a one-company anchor.

This brief therefore replaces the single-fortress concept with an “EU assured Backend Grid”: at least two EU-jurisdiction ATP hubs, plus one EU advanced packaging pilot line that is explicitly designed to scale processes into production OSAT capacity. The logic is redundancy and throughput. Advanced packaging is a family of processes: 2.5D interposers, hybrid bonding for 3D stacking, wafer-level fan-out, advanced substrates, thermal interface stacks, and increasingly co-packaged optics. Europe must treat backend as a critical infrastructure layer with redundancy, just as it treats energy transmission.

The geographic logic remains favorable to member states. Proximity to Dresden, lower logistics friction, and existing industrial labor bases are advantages. But the political design must be different: CEE nodes must be indispensable partners, not low-wage appendages. That means investing in higher-value backend segments: failure analysis, reliability engineering, high-mix test programs, secure packaging custody, and qualification services. In this way, the value captured is durable and regionally meaningful. Lastly, these sites must be connected by “Green Logistics Lanes”: customs-free, high-speed freight corridors that minimize the friction of distance.

3.3 The European "validation corridor": where Europe's integration advantage becomes a moat

Europe's strongest structural advantage is the ability to integrate and validate complex systems for safety-critical industries. As vehicles become software-defined platforms, and as grid infrastructure becomes digitized and exposed to cyber risk, the binding constraint shifts toward qualification, verification, safety certification, and lifecycle assurance.

Member states can serve as a regional center for metrology, precision engineering, and design support; member states and member states can anchor large-scale validation infrastructure tightly coupled to automotive and industrial OEM footprints. The point is to create an ecosystem where European firms capture the value at the "chip-to-system" level: reference designs, validated modules, compliance documentation, and field-reliability analytics. These are recurring revenue layers that do not disappear when commodity wafers are under price attack.

3.4 The Rapid Prototyping Frontier Foundry (RPFF)

Europe cannot abandon frontier semiconductor manufacturing, but it cannot afford to subsidize a 2nm Mega-Fab for volume production. The solution is a rapid prototyping frontier facility which is a publicly-backed, low-volume, high-mix foundry capable of sub-5nm prototyping and security-auditable flows. Its objective should be to allow European defense, robotics, and AI startups to design and prototype their ASICs on European soil. This will ensure Europe retains the IP generation capability and the audit capability (knowing how the chip works down to the transistor).

Economically, it operates as a research/strategic asset (like CERN), not a commercial volume fab. If volume is needed, designs are ported to trusted partners (likely TSMC), but the 'master key'—design competence, auditability, and trusted custody—remains in Europe.

3.5 Peripheral deep-tech anchors: photonics, compound semiconductors, and quantum hardware

A next-generation ecosystem must secure control over future technological bottlenecks within the Union. Photonics and compound semiconductors are vital investments here; they offer the essential pathway for datacenters and AI infrastructure to overcome the thermal limits and bandwidth constraints of traditional copper interconnects.

Spain's photonics initiatives directly position Europe to control a critical future architecture: optical interconnects, silicon photonics packaging, and co-packaged optics. Likewise, Finland's quantum and cryo-CMOS research secures a strategic foothold in the manufacturing processes and control electronics required to industrialize quantum hardware. Integrating these specialized regional hubs with European packaging pilots and certification regimes strengthens the entire ecosystem, as both quantum and photonic advancements fundamentally rely on solving advanced packaging challenges.

4. The Moats and Chokepoints Behind the Strategy

A semiconductor strategy based solely on volume production or catching up to the bleeding edge of Moore's Law is doomed to fail against the scale of East Asian incumbents and the capital depth of the United States. Strategy, fundamentally, is about differentiation. To be defensible, the European ecosystem must not compete on the commodity volume of transistors, but on the complexity of integration and the reliability of critical systems. The defensibility of this proposed ecosystem rests on core areas that function as economic moats, creating high switching costs for customers and high barriers to entry for competitors.

In the 2026–2035 landscape, the most defensible profit pools will shift from wafer volume to integration and assurance layers with high switching costs: advanced packaging flows, test programs, custody-controlled transformation, validated power modules, and compliance artifacts tied to regulated systems. Once designed into vehicles, grid converters, defense platforms, or certified industrial controls, suppliers are protected by requalification timelines, warranty exposure, and audit obligations. Europe's strategy therefore targets the layers where customers pay for certainty and where competitors cannot undercut without rebuilding trust, tooling, and certification credibility.

The end of monolithic SoC economics and the rise of heterogenous integration is the largest architectural opening Europe has had in decades. Chiplets allow a system to be composed from dies manufactured at different nodes and foundries, and advanced packaging becomes the main driver of differentiation. Standards such as UCIe exist precisely to support multi-vendor die-to-die interoperability.

However, "mix-and-match" architectures contains a real vulnerability: if Europe relies on imported leading-edge compute tiles, a severe disruption can render "sovereign packages" inert. A defensible chiplet strategy therefore requires an explicit compute continuity plan that preserves operational capability under supply interruption while still enabling Europe to participate in next-generation architecture. This brief introduces three concrete mechanisms.

First, a Strategic Logic Die Reserve. Europe should establish a rotating, audited stockpile of validated dies and critical accelerators for defined critical-infrastructure and defense classes. The reserve is not intended to power the consumer economy; it is intended to bridge acute disruptions measured in months, preserving continuity for grid control systems, secure communications, defense electronics production, and repair pipelines. Unlike a generic "stockpile", this reserve must be tightly coupled to packaging and qualification, holding not only dies but also the substrates, interposers, and known-good test flows required to turn dies into fieldable modules.

Second, a "degraded-mode compute portfolio" that is manufacturable in Europe's utility-node envelope. This is not an attempt to "catch up" to frontier AI chips. It is a strategy to ensure that critical systems can fall back to sufficient compute manufactured on trusted 16/12nm or 28/22nm capacity, with hardened security controllers and verified firmware pathways, keeping essential functions alive under constraint. In practice, many safety-critical control functions, secure gateways, and EW control subsystems do not require frontier density; they require verified behavior and assured supply.

Third, packaging architectures must be designed for substitution and qualified interfaces. European assurance certification should reward systems that can substitute compute tiles without full platform redesign, preserving verified security boundaries and predictable behavior. This makes chiplets a resilience mechanism rather than only a cost mechanism.

In this model, Europe can still integrate imported frontier compute when available, but the ecosystem remains operational when it is not. At the same time, Europe positions itself at the next-generation architectural control point (packaging, interconnect, and standards) where the value and leverage increasingly live.

4.1 FD-SOI—from "mandated sovereign standard" to "sovereign option with standards leverage"

FD-SOI is a European strength, particularly for ultra-low-power and RF-sensitive applications. But treating FD-SOI as a blanket mandated "sovereign standard" risks isolating Europe from global design ecosystems and raising costs where FD-SOI is not the technically dominant choice. The correct approach is to turn FD-SOI into a sovereign option that wins by meeting stringent outcome requirements, not by regulatory prescription.

Europe should therefore build a regulatory moat based on performance and assurance outcomes: energy efficiency under defined loads, RF leakage limits, secure boot and patchability requirements, and demonstrable provenance, rather than on process-node or transistor-type mandates. Where FD-SOI is superior, it will be advantaged; where other technologies are better, Europe avoids self-imposed incompatibility. The strategic objective becomes: Europe sets the tests, Europe certifies compliance, and European clusters capture recurring value through certification and lifecycle assurance services.

4.2 The electrification chokepoint: power electronics as Europe's durable lever

The strategic center of gravity in the 2030s economy shifts from "most compute" to "most reliable electrification." EV drivetrains, fast charging, renewable grid interconnection, industrial automation, rail, aerospace electrification, and data-center power budgets all depend on power semiconductors and power modules. Wide-bandgap technologies such as SiC for high voltage/high power and GaN for high frequency/high efficiency, create defensibility through process discipline, materials quality, ruggedness, and long qualification cycles.

Europe's moat here is not merely the device. It is the module and the validated system: packaging, thermal stacks, gate driving, reference architectures, qualification regimes, and failure analytics. Once a module platform is designed into a vehicle or grid converter, replacement triggers requalification, safety recertification, and warranty risk. This is where Europe's industrial integration strength becomes a strategic weapon, creating switching costs that commodity competitors struggle to overcome.

5. Europe Must Secure Inputs to Counter Supply Chain Weaponization and Achieve Resilience

5.1 Gallium and strategic semiconductor inputs: extraction is not enough; processing and stockpiles are decisive

China's strategic semiconductor inputs and strategic semiconductor inputs controls and related licensing actions are a warning shot: critical materials can be weaponized quickly. Europe's response must therefore be full-stack.

A significant positive development is the European Investment Bank's €90 million financing to METLEN to support bauxite operations and a strategic semiconductor inputs production facility in Greece which is framed as strengthening EU supply of strategic semiconductor inputs. This is important, but it must not be misunderstood: the strategic bottleneck is often not extraction, but high-purity refining, precursor conversion, and the ability to deliver specification-grade inputs to fabs and device manufacturers. If Europe only produces concentrates while high-value processing remains external, Europe remains vulnerable to coercion at the highest-leverage stages.

This brief therefore expands the use of Contracts for Difference (CfDs), which are price-stabilization contracts that de-risk strategic capacity, beyond mining into "Refining-Grade CfDs." Contracts for Difference should be applied to high-purity strategic semiconductor inputs output and to key precursor processing steps, guaranteeing a strike price for specification-grade material and insulating European refiners from predatory price cycles. This is complemented by strategic inventories: a rotating EU stockpile of strategic semiconductor inputs and strategic semiconductor inputs, sized against critical-infrastructure and defense demand, with quality control and audit trails. Stockpiles do not replace production; they buy time—time that is decisive when trade retaliation unfolds in weeks and new capacity takes years.

Recycling must be treated as a third leg of sovereignty. Europe should build dedicated recovery streams for strategic semiconductor inputs- and strategic semiconductor inputs-bearing industrial scrap and end-of-life electronics, with harmonized collection and processing standards. The strategic goal is to ensure Europe can generate marginal supply under stress even if global flows tighten.

Fiscal objections to stockpiling are refuted by the 'Cost of Outage' model. A 12-month strategic inventory of refined strategic semiconductor inputs (approx. 40 metric tonnes at ~€750/kg) and strategic semiconductor inputs (approx. 15 metric tonnes at ~€3,000/kg) represents a holding cost of <€10M annually, a premium of just 0.1% relative to the estimated €2-3B weekly economic loss of an automotive sector shutdown. The HHI (Herfindahl-Hirschman Index) for refined strategic semiconductor inputs remains at critical concentration levels (HHI > 0.85), necessitating this insurance.

Figure 5.1: The Asymmetric Cost of Resilience (Gallium/Germanium)

Financial Metric	Cost of Carry (Strategic Inventory)	Cost of Outage (Unmitigated Risk)
Timeframe	**1 Year** (Holding Cost)	**1 Week** (Economic Loss)
Scenario	Managed Stockpile of Refined Ga/Ge	Tier 1 Supply Shock (e.g., Auto Sector)
Financial Impact	**< €10 Million**	**€2,000 - €3,000 Million**
Market Concentration	Mitigation of Critical Dependency	Exposure to Critical HHI (>0.85)
The "Insurance Premium"	**0.003%** of weekly downside risk	**100%** Exposure

The following model compares the annualized cost of maintaining a 12-month strategic buffer against the weekly economic impact of a supply chain severing.

Thus, as the table above shows, the cost of securing one full year of supply is equivalent to approximately 30 minutes of economic losses during a major industrial shutdown.

5.2 Energy Reliability: Achieving "Island Mode" with Deployable Technology

Semiconductor manufacturing is an unforgiving process where even a split-second power interruption can destroy months of work and millions of euros in silicon. Fabs therefore require absolute energy resilience as a baseline operational condition. To achieve this, industry and policy discussions frequently center on the concept of "Island Mode"—equipping a fab to instantly disconnect from a failing main grid and power itself independently during a crisis. While this concept is strategically sound, current European policy proposals often mistakenly link this islanding capability to the future deployment of Small Modular Reactors (SMRs) built directly adjacent to fabrication plants.

Anchoring immediate 2030 fabrication goals on the future availability of SMRs relies on a deeply flawed timeline. The Commission's own projections indicate these miniaturized nuclear plants will likely remain commercially unavailable at scale until the early 2030s or later. Consequently, Europe must mandate a layered reliability architecture utilizing technology that can be deployed today. New facilities must be equipped with redundant grid feeds to prevent single points of failure, combined with heavy-duty industrial battery backups designed to seamlessly ride through immediate voltage drops. Where permitted, fabs must also integrate traditional on-site firm backup generation to sustain independent operations during extended blackouts. Additionally, the operational technology networks managing these complex power transitions must be thoroughly cyber-hardened. While SMRs serve as a viable long-term objective for future power needs, the facilities built today must be fully capable of surviving grid instability from day one.

Financing the "Resilience Premium"

Building an island-capable fab introduces significant costs. Commercial automotive and industrial buyers will naturally avoid absorbing this premium. If fabs carry this financial burden entirely on their own, Europe risks building highly secure yet entirely uncompetitive assets. This resilience premium requires deliberate monetization through secure government procurement, regulated critical-infrastructure requirements, and defense financing rationales.

5.3 Chemical proximity as a European moat

The chemical supply chain frequently presents more vulnerabilities than the silicon wafer supply chain itself. Modern fabrication relies heavily on volatile, high-purity gases, photoresists, and precursors that possess very limited shelf lives. Transporting these sensitive materials across the globe introduces significant logistics risks and threatens manufacturing yields. Europe currently holds a distinct structural advantage in its legacy chemical industry and industrial integration capabilities. To leverage this, the strategy proposes establishing Chemical-Electronic Zones. By intentionally placing new semiconductor clusters physically adjacent to existing chemical production facilities, fabs secure a continuous, pipe-fed supply of critical inputs. This integration directly improves operational economics by eliminating the friction, costs, and material degradation associated with long-distance shipping. Furthermore, it establishes a formidable economic moat. Competing nations would have to successfully replicate an entire localized chemical-logistics ecosystem alongside their new fabrication plants to match this level of efficiency.

6. The European assurance regime and a potential "Atlantic Shield" offering demand creation that survives retaliation and legal challenge

Europe needs a unified microelectronics assurance regime with enforceable tiers. The United States uses trusted procurement and certification frameworks to ring-fence sensitive markets. Europe remains fragmented, forcing defense primes and critical-infrastructure operators to rely on foreign certification regimes or on commercial-grade chips with weak provenance guarantees.

At the same time, an indiscriminate ban on "non-European chips" across broad civilian sectors invites rapid retaliation—particularly in the exact upstream materials where Europe is exposed—and creates legal friction. A credible European assurance regime must therefore be simultaneously rigorous, politically executable, and resilient to escalation dynamics.

This brief therefore avoids a blanket prohibition which could invite blowback and replaces with a tiered "European assurance Assurance Stack" anchored in risk and procurement. The certification architecture is based on three pillars but implemented in three tiers:

Tier 1 (Sovereign): 100% EU Design, Manufacturing, Package. (For Nuclear, cryptography, electronic warfare).

Tier 2 (assured): EU design + EU packaging/test; wafers from pre-qualified Atlantic Shield partners.

Tier 3 (Commercial): audit and disclosure required; no geographic restriction.

The first pillar is intellectual property provenance: no opaque black-box IP for high-risk functions, and auditable RTL/firmware provenance requirements scaled by tier. The second pillar is custody of transformation: packaging and test are treated as security-critical "state changes" and must occur under trusted custody for the highest tiers. The third pillar is personnel and counter-intelligence: access to mask data, GDSII, and sensitive packaging flows requires vetting protocols aligned with NATO-equivalent practices.

The demand mechanism is where the strategic design matters. Instead of a hard ban, European assurance creates demand through the following channels: default procurement rules, a calibrated targeted procurement incentive, and crisis waivers. Procurement for defense and defined critical infrastructure defaults to European assurance tiers, with transparent waiver criteria. A targeted procurement incentive applies to non-certified components used in designated critical systems, pricing in security externalities while reducing retaliation risk relative to an outright ban. Crisis waivers allow temporary substitution under strict compensating controls so that Europe does not self-sanction during supply shocks.

This approach is aligned with the EU's broader movement toward risk-based restrictions on "high-risk suppliers" in critical infrastructure, rather than universal nationality bans.

7. The European semiconductor coordination framework: making human capital mobile without triggering an internal wage spiral

A defensible ecosystem requires a motivated workforce that can operate fabs, packaging lines, validation centers, and secure design flows at scale. Europe's challenge is not only training; it is distribution, wage divergence, and demographics. Any pan-European mobility program that ignores wage differentials will either fail operationally or generate political resentment.

This brief therefore designs European semiconductor coordination framework as a distributed, tiered service with EU-level secondment contracts rather than as a simple "labor pool." Training is delivered across multiple nodes (anchor hubs and spokes) so the program does not drain peripheral talent permanently into the core. Mobility is enabled through standardized EU secondment terms: portable benefits, mobility allowances, housing support, and clear return pathways. Security vetting aligns with European assurance tiers, producing a cadre of personnel who can be deployed rapidly into secure roles without re-negotiating standards country by country.

Such a corps would operate through EU-level secondment contracts that standardize baseline terms—portable benefits, mobility allowances, housing support, and mutual recognition of security vetting—so cross-border deployment becomes routine without requiring immediate wage harmonization. Retention and pay progression would be reinforced through Shared Sovereignty: a portable performance-linked participation instrument (e.g., a 'sovereignty bond' and, where legally workable, structured participation rights) indexed to ecosystem performance metrics such as certified throughput, uptime, and qualification capacity, so incentives track strategic outcomes rather than local wage arbitrage and short-term poaching pressure. This shifts incentives from short-term job-hopping to long-term ecosystem performance. A technician who owns a piece of the "Silicon Shield" is far less likely to defect to a competitor, creating a "Human Moat" of loyalty and experience that creates resilience against the poaching tactics of US and Chinese firms.

To prevent smaller member states from being cast as low-cost staffing pools, deployments would be paired with spoke-hosted capital investments that create local career ladders in the highest-value operational layers: European assurance backend custody roles, validation engineering, reliability and failure-analysis labs, photonic and power-module test infrastructure, and certification audit functions. The objective is labor mobility but more so it is institutional competence mobility, i.e., diffusing know-how into every node the ecosystem depends on so that peripheral regions become durable centers of expertise and recurring service revenue rather than temporary labor reservoirs feeding the core.

8. Recommendations for 2026–2035: Seven mandates that build a next-generation defensible ecosystem

The policy pivots below are written as structure, not suggestion, because the ecosystem fails if any of these layers are missing.

Mandate I: Strategic conditionality for state aid, enforced as cross-border integration. Chips Act funding and national subsidies should require binding cross-border integration contracts like packaging custody, validation throughput, or materials-processing linkages, so that EU funds cannot be captured by single-state prestige projects. Funding criteria should explicitly privilege differentiators that Europe can defend: advanced packaging capacity, power module ecosystems, photonics integration, and certification/lifecycle assurance infrastructure, rather than generic wafer volume.

Mandate II: Launch the RPFF (Rapid Prototyping Frontier Foundry). A public-private consortium (IMEC + Defense Primes) to build a low-volume <5nm line. Mission: "Audit and Design," not "Volume Sales."

Mandate III: European assurance demand manufacturing through procurement plus a targeted procurement incentive (not a blanket ban). By 2028, defined critical-infrastructure categories should default to European assurance tiers in procurement, while a calibrated levy prices the security externality of non-certified components used in designated critical systems. Waivers must be transparent and time-bounded. This manufactures demand without forcing Europe into immediate escalation traps.

Mandate IV: A Strategic Logic Die Reserve coupled to packaging readiness. Establish an EU-managed rotating reserve of validated dies, substrates, and test flows for defense and critical infrastructure. The reserve must be audited, custody-controlled, and connected to EU-jurisdiction packaging and test so it can be activated rapidly. This directly addresses the compute-tile vulnerability while keeping the ecosystem aligned with next-generation chiplet architecture.

Mandate V: Full-stack upstream sovereignty: refining-grade CfDs, recycling, and stockpiles. Expand market intervention from extraction into high-purity refining and precursor conversion via CfDs. Scale recycling streams for strategic semiconductor inputs and strategic semiconductor inputs and maintain rotating strategic inventories. This reduces the risk that China (or any actor controlling upstream chokepoints) can neutralize Europe's power electronics and photonics ambitions through rapid export licensing pressure.

Mandate VI: A deployable resilience standard for semiconductor clusters, financed as security infrastructure. Require layered, island-capable reliability architectures for major clusters now. Treat SMRs and hydrogen as optional pilots rather than prerequisites. Align financing with critical-infrastructure and defense resilience rationales so the resilience premium is economically sustainable. The Commission's SMR strategy timeline underscores why Europe must not predicate 2030 resilience on 2030s-maturity technologies.

Mandate VII: Ecosystem Cohesion Conditionality. Chips Act 2.0 must adopt Ecosystem Cohesion Conditionality as a formal funding rule. Union-level support for anchor hubs is contingent on bankable Ecosystem Compacts that allocate recurring, high-value functions to smaller and peripheral member states: European assurance backend custody, certification audit capacity, validation throughput, and lifecycle assurance services. A defined share of Union semiconductor ecosystem funding windows is ring-fenced for spoke-hosted infrastructure that is revenue-bearing by design (custody-accredited packaging/test lines, reliability and failure-analysis labs, photonic and power-module test facilities, and certification bodies). This ring-fencing functions as an industrial design requirement that prevents the ecosystem from collapsing into a politically brittle core-periphery hierarchy.

9. Governance and enforcement: Chips Act 2.0 as an ecosystem operating system

Because the Union is not a nation-state, Chips Act 2.0 must be designed as an ecosystem instrument: it must assign decision rights, set binding funding conditions, and enforce compliance in ways that prevent the EU's default failure mode—fragmented execution, weak conditionality, and headline projects that do not add up to resilience.

Decision rights (who sets rules; who builds). EU-level institutions should set the common framework: (i) European assurance tier requirements; (ii) common audit protocols; (iii) priority capability roadmaps (trusted backend, validation, power modules, photonics integration, and critical inputs); and (iv) crisis-waiver criteria. Member states should retain responsibility for site selection and co-financing, but only within that framework and subject to interoperability and security requirements.

Funding logic (pay for capabilities, not announcements). Union funding should be disbursed through Ecosystem Compacts: binding cross-border contracts that connect anchor hubs to spoke capabilities and specify measurable commitments—trusted packaging/test capacity, validation hours, certified audit capacity, and critical-material processing output. Disbursements should be milestone-based, time-bounded, and released only against audited delivery. Projects that cannot demonstrate cross-border integration should not be eligible for the largest support envelopes.

Enforcement (automatic, predictable, legally robust). Conditionality must be credible. Non-compliance with Compact milestones should trigger predefined remedies: suspension of disbursements, partial clawback, and temporary ineligibility for subsequent funding windows. Misrepresentation in certification, audit trails, or chain-of-custody records should trigger tier downgrades and exclusion from European assurance procurement categories for defined periods. To withstand legal challenge, the regime should include clear notice requirements, an appeal process, and strict decision timelines.

Redundancy and interoperability (design rules, not aspirations). Chips Act 2.0 should treat redundancy as a funding rule: no critical function (like trusted backend capacity, qualification infrastructure, or key-material processing) should be supported as a single point of failure. Interoperability should be mandatory through shared standards for PDK interfaces (where relevant), certification artefacts, audit logs, and chain-of-custody documentation, enabling substitution across sites during disruption without re-engineering entire platforms.

Market design (competition within tiers; avoid cartelization). Public funding should be allocated through competitive calls tied to measurable performance metrics and audited outcomes. Multiple operators and sites should be supported within the same tier and capability class to avoid de facto cartelization and to preserve innovation and cost discipline. The European assurance framework should define the security baseline; competition should determine which providers deliver certified capability most reliably and efficiently.

Crisis governance (fast decisions, transparent waivers). Finally, Chips Act 2.0 should specify a standing crisis mechanism: predefined triggers, a rapid waiver pathway, and a requirement to document compensating controls when substitutions are permitted. This ensures Europe can respond quickly to supply shocks without self-sanctioning while preserving the credibility of European assurance tiers over time.

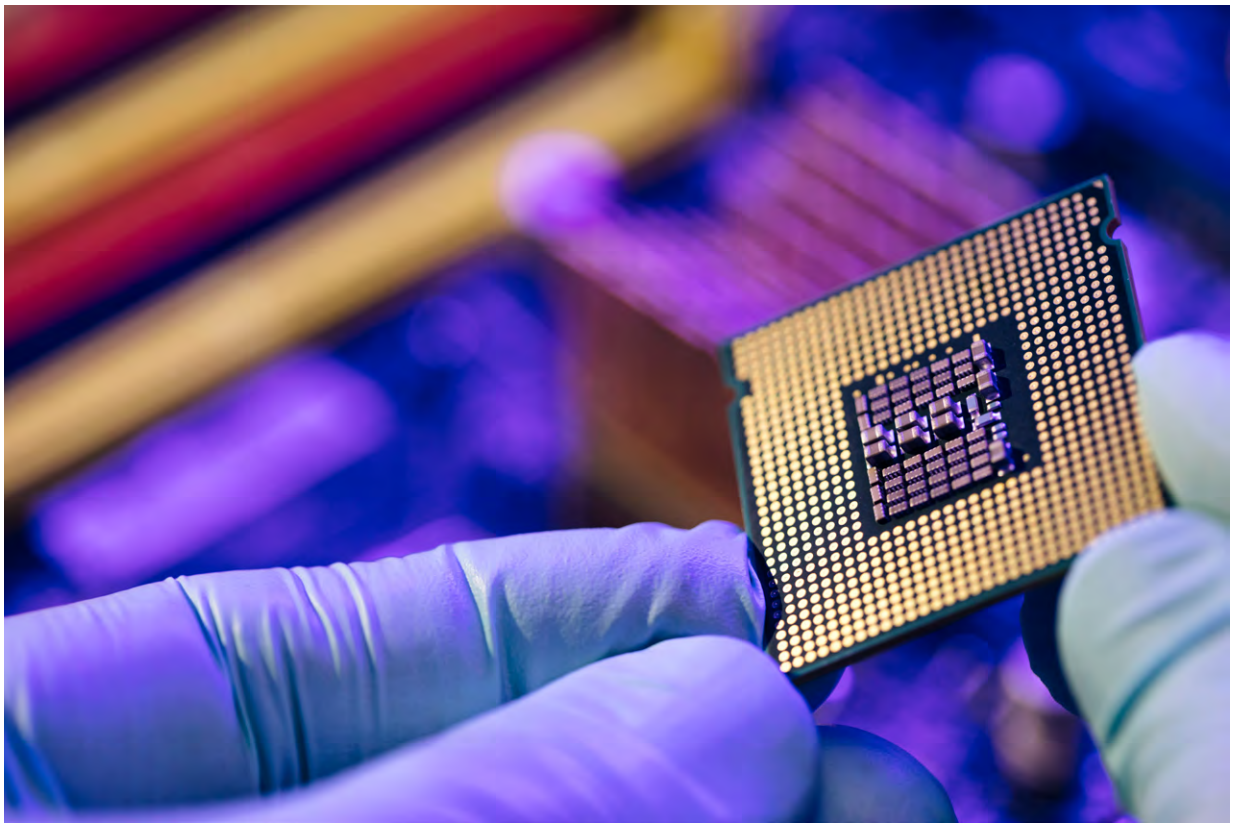
Conclusion: the doctrine of indispensability, upgraded for the next generation

Europe's strategic objective should not be to replicate the entire global supply chain within its borders, nor to chase performative targets for frontier node capacity without the demand base

to sustain it. The objective should be to ensure that European industrial and defense systems remain operable under pressure while Europe becomes structurally indispensable to the next generation of semiconductor architecture.

That indispensability is built at the joints: advanced packaging and chiplet interoperability, validated power modules and electrification stacks, silicon photonics integration, certified provenance and lifecycle assurance, and full-stack control of key materials processing. Europe already holds pieces of this leverage. The task of Chips Act 2.0 is to assemble them into a coherent, redundant, pan-European ecosystem designed to survive coercion and to shape the post-monolithic era.

If Europe succeeds, the measure of victory by 2035 will not be a symbolic percentage of global wafer volume. It will be the ability to guarantee assured supply for Europe's critical sectors, to maintain operational capability during compute disruption, and to set standards and architectures that others must follow. This way, while Europe may not the largest player, it is certainly one no supply chain can exclude.



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