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The Fab is Not Enough: An Asymmetric Semiconductor Strategy for European Sovereignty

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Executive Summary

The era of the free-market microchip is permanently dead. Today, semiconductors are the apex weapons in a new age of fierce techno-nationalism. An industry once governed by efficiency-driven, globalized supply chains is increasingly shaped by geopolitical pressure, export controls, and industrial policy interventions, re-emerging as the primary battlefield for geopolitical, economic, and military dominance. We have entered an arena of intense techno-bloc rivalry where semiconductors are the central prize. For the European Union, treating this new reality as a mere industrial policy challenge is a category error that guarantees failure.

In this new era, the European Union finds itself in a position of profound strategic vulnerability. The continent consumes approximately 20% of the world's chips but produces less than 10%. This deficit is acute in advanced logic, where a near-total dependency on East Asia for the sub-7nm chips that power modern economies, artificial intelligence, and military systems constitutes a critical national security threat. This dependency is a structural deficit that exposes the continent to catastrophic supply chain shocks and subordinates its strategic autonomy to the foreign policy decisions of other global powers.

The European Chips Act, which entered into force in September 2023, represents one of the most significant industrial policy interventions in the Union's history. It is a strategy born from a profound "Chance" event that saw the convergence of the COVID-19 pandemic and subsequent geopolitical shocks, which exposed a critical dependency on foreign-made chips. The resulting supply chain collapse cost the European economy, by one senior German official's estimate, between 1-1.5% of its GDP in 2021. The Act, mobilizing €43 billion in public and private investment, correctly identifies and attempts to leverage the EU's powerful strengths, which include its world-class R&D ecosystem centered around institutes like IMEC and Fraunhofer and its globally monopolistic position in lithography via ASML.

However, the Act's execution, particularly under its second pillar (Security of Supply), fundamentally deviates from the requirements of creating sustainable, innovation-driven advantage. It substitutes massive, government-led subsidies for foreign firms and mandated "co-opetition" among domestic players for the intense domestic rivalry that is the true engine of national competitiveness. As such, it misdiagnoses the fundamental problem. Europe's weakness is certainly a lack of factories, but its ultimate vulnerability is a lack of sovereign control over the most critical, value-generating segments of the industry and an absence of the sophisticated domestic demand and rivalry needed to foster leading-edge champions.

Thus, Europe's current strategy, fixated on a "catch-up" race to achieve an arbitrary 20% global production share, is failing. As noted by the European Court of Auditors (ECA) in its 2025 report, this target is "deeply disconnected from reality" and "overly ambitious". Europe cannot and should not attempt to replicate the entire value chain.

Instead, its strategy must be asymmetric. This paper advocates for a disciplined and ruthless pivot: abandon the metric of total output and focus all resources on becoming the system architect of the global chip order. The objective is the creation of Europe's own indispensable chokepoints in the global supply chain. By achieving dominance in these targeted areas, Europe can transform its current dependency into a position of mutual, balanced interdependence with its allies, particularly the United States, in an environment of low political trust.

By 2035, Europe will leverage its unique and non-replicable chokepoints in equipment and materials to secure trusted access to leading-edge manufacturing, dominate strategic niche markets like power and automotive, and co-write the global rules for a resilient, secure, and sustainable semiconductor ecosystem. The vision is deterrence by interdependence, making Europe indispensable to allies and adversaries alike.

This paper proposes a new grand strategy, a **"Strategic Silicon Framework (SSF)."** To achieve this, we outline a comprehensive 10-pillar execution plan (detailed in Section VI) that drives toward six strategic imperatives:

Imperative 1: Secure and leverage core assets. Treat EU tool, optics, and substrate champions as strategic infrastructure. Co-fund High-NA EUV, hybrid bonding, and ALD for backside power. Crucially, align export policy at the EU level in exchange for reciprocal foundry access and crisis priority guarantees.

Imperative 2: Assure leading-edge access, not copycat scale. Make the ESMC model the strict condition for large fab aid. Require EU anchor customers with long-term off-take agreements and embed crisis priority clauses for EU/NATO demand in every award.

Imperative 3: Own post-silicon bottlenecks. Build two to three advanced packaging megahubs for 2.5D and 3D integration, chiplets, photonics, and trusted packaging. Tightly link manufacturing to imec, Fraunhofer, CEA-Leti, and European equipment houses to accelerate pilots into qualified products.

Imperative 4: Win strategic niches. Double down on SiC and GaN power, automotive and industrial MCUs, sensors, and secure elements. Use EU procurement and standards to hardwire demand, measuring success by global profit pool share rather than mere volume.

Imperative 5: Make defense the anchor customer. Treat chips as ammunition. Fund trusted, long-lifecycle capacity inside EU fabs and packaging sites for radiation-hardened, secure, and traceable parts. Build a common EU defense chiplet library and embed semiconductor stress scenarios into NATO and EU exercises, backed by a strategic stockpile.

Imperative 6: Enforce execution, workforce, and cost discipline. Establish a European Semiconductor Facility to mobilize €80–€120 billion through 2035. Tie every major award to strict conditions: long-tenor low-carbon power contracts, 80% water reuse by year three, on-site train-to-hire academies (20k–30k hires/year), and anti-cannibalization safeguards for existing EU talent.

Concrete 2035 Outcomes Successful execution of these imperatives will result in:

One continuously upgraded leading-edge logic/AI complex (2nm class and below) in the EU, built on the ESMC model with guaranteed EU/NATO crisis-priority rights.

Two to three advanced packaging megahubs covering 2.5D/3D stacking, secure packaging, and photonics, anchored by projects like Silicon Box and allied co-ownership.

Dominant global profit-pool share in strategic niches: SiC/GaN power, automotive/industrial MCUs, sensors, and secure elements.

A permanent European Semiconductor Security Council (ESSC), formalizing the 2025 "Semicon Coalition" with binding coordination powers across funding, export controls, and crisis allocation.

A European Semiconductor Facility (ESF), consolidating fragmented national/EIB funds into a unified €80–€120 billion blended finance engine.

I. Semiconductors As Statecraft

The defining feature of the 2025-2035 era is the structural bifurcation of the global technology ecosystem. The rivalry between the United States and China has morphed beyond cyclical trade disputes into a full-scale technological and economic cold war. In this new conflict, semiconductors are the primary instrument of statecraft, supplanting 20th-century oil dependency as the new "gravity well" of national power.

States now openly use access to semiconductor technology to strengthen national security, gain economic leverage, and alter the global balance of power. This rise of techno-nationalism forces all other powers, including Europe, into an alignment.

> Neutrality in the trade of strategic technologies is no longer a viable option, as export control regimes and investment screening are now primary, offensive tools of foreign policy.

Nowhere is this more acute than in the military domain. Semiconductors are the cognitive engine of modern warfare, enabling the precision of guided munitions, the sensing capabilities of advanced radar, the security of encrypted communications, the effectiveness of electronic warfare, and the cognitive edge provided by artificial intelligence (AI) in command and control. A nation or bloc that cannot guarantee its access to a secure, trusted supply of these chips cannot guarantee its military autonomy. Its capacity for self-defense and its ability to project power are fundamentally compromised, and thus subjected to the strategic interests of foreign suppliers.

The EU is no longer an observer of this conflict; it is a contested territory within it.

U.S. statecraft and the "ASML card." Washington is running a degrade strategy against China's military-civil fusion by tightening access to advanced compute. That strategy reaches Europe through controls on ASML. The United States pressed The Hague to stop shipments of EUV systems to China and to narrow exports of certain DUV tools. The Netherlands has reasserted national licensing authority on specific models, yet U.S. EAR rules still bite. ASML must track U.S. rule changes in real time, which blurs the line between Dutch sovereignty and American extraterritoriality.

China's counter-leverage. Beijing has shown it holds its own chokepoints. It imposed export controls on gallium and germanium, inputs that sit at the core of compound semiconductors and sensing. It also opened anti-dumping probes into European and U.S. analog producers, a direct shot at mature-node supply chains that feed Europe's automotive and industrial base.

Russia's upstream pressure. The war in Ukraine exposed dependence on Russian palladium for plating and packaging and on neon for excimer lasers in DUV lithography. The initial shock was sharp. European firms have since diversified and increased recycling, but the episode proved how easily upstream materials can ripple through the entire chain.

Europe is not setting the rules in this environment; it is reacting to them. The clearest recent case is the 2025 Nexperia crisis, which showed that even when wafers are produced on European soil, control over offshore assembly and test can halt deliveries to Europe's largest industries in a single stroke.

Nexperia 2025: Lessons in Hidden Dependence

Europe's semiconductor problem goes much deeper than advanced chips from Taiwan. As the Nexperia crisis last year highlighted, there's an equally dangerous reliance on China just to package older, mature chips.

The Asset: Nexperia, a major global producer of "legacy" discrete and analog chips, is Chinese-owned (via Wingtech Technology) but is headquartered and operates a key fab in the Netherlands. These chips are indispensable for the European automotive industry, used in everything from airbags to power steering.

The Conflict: In late September 2025, the Dutch government, citing national security concerns and U.S. pressure, seized control of Nexperia

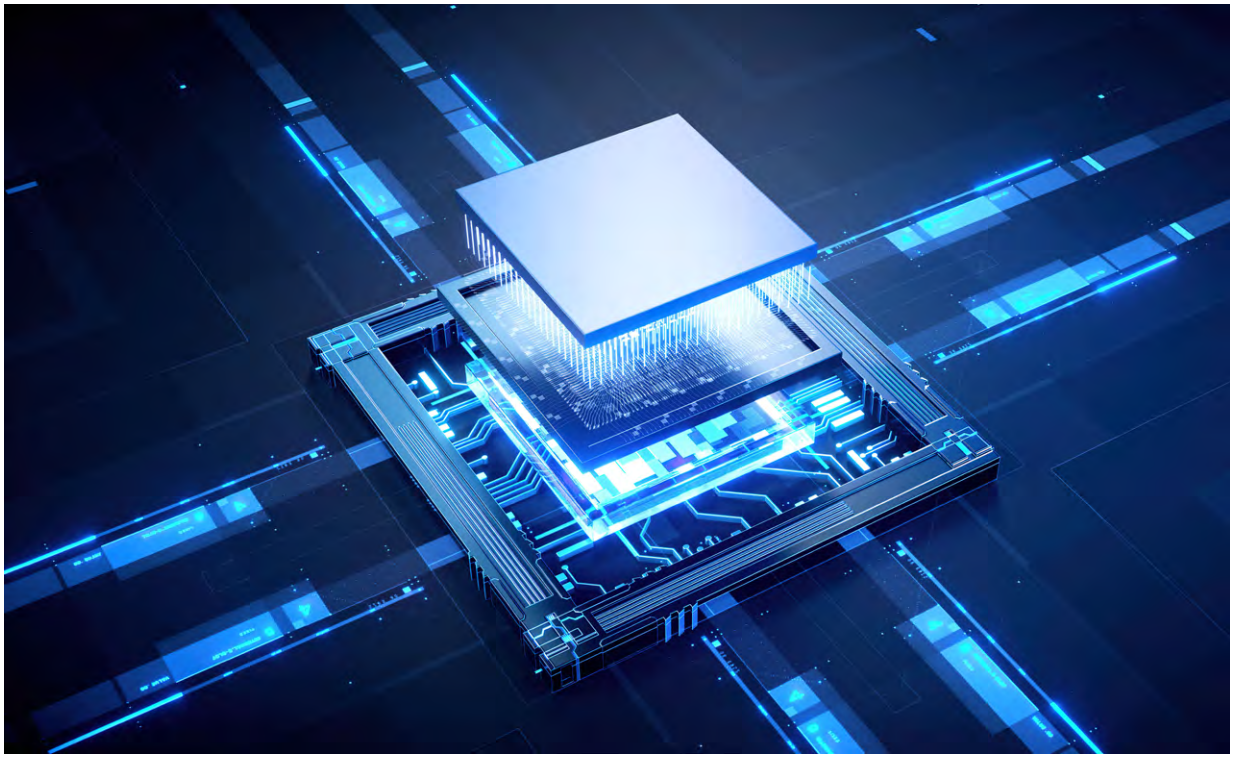
to prevent technology transfers and production relocation.

The Retaliation: Beijing's response was swift and asymmetric. In October 2025, it banned exports of Nexperia products from its packaging and assembly facilities within China. While the wafers were fabbed in Europe, Reuters reports that around 70% were packaged in China, creating a fatal chokepoint.

The Impact: The result was an immediate, acute supply crisis for European industry. Major automakers, including Volkswagen and Stellantis, warned of imminent production shutdowns. The crisis demonstrated that a European industrial asset could be neutralized by a foreign power's control over a "low-value" downstream step.

The Resolution: The crisis was only resolved by a "presidential-level" diplomatic intervention, culminating in a broader U.S.-China trade deal in November 2025 that saw both sides de-escalate, with Beijing granting temporary exemptions and allowing the flow of chips to resume.

The Nexperia crisis is a third-order lesson: Europe's dependency is multi-layered. Control of a fab is useless if another power controls the packaging. This event validates the imperative to secure the entire value chain for critical components, from materials (Pillar IX) to packaging (Pillar IV).



II. Europe's Exposure

The 2025 Nexperia crisis was an escalation, but the "unraveling moment" came in 2020. The COVID-19 pandemic fired the first warning shot, acting as a global stress test that revealed the fundamental fragility of the "just-in-time" semiconductor value chain. The resulting "chip shortage" was widely misdiagnosed at the time as a temporary supply chain glitch. The deeper, more permanent truth was that it represented a structural power shift. Europe's industrial champion, the automotive sector, discovered with bruising speed that it was a low-priority, low-margin customer for Asian foundries. Automakers, anticipating a slump, cancelled their chip orders. When demand quickly rebounded, foundry capacity had already been allocated to higher-margin, higher-volume customers in the consumer electronics and data center sectors. The shortage was not only a supply problem but also a leverage problem. In a capacity-constrained world, Europe's most important and sophisticated industry lacked the market power to secure its own supply chain.

This lack of leverage had catastrophic and quantifiable costs. The political will for the European Chips Act was born from this economic trauma. As a senior German official observed in 2023, the shortage "lost 1-1.5 percent of our GDP in 2021... or about €40bn" for Germany alone.

This economic shock was the direct result of a structural deficit, decades in the making.

> Europe's share of global semiconductor manufacturing has collapsed from nearly 40% in 1990 to under 10% today. This is a fraction of its ~20% share of global consumption.

This hallowing out of industrial capacity represents three decades of strategic atrophy, a deliberate offshoring of production in pursuit of globalized efficiency that has now become a critical vulnerability. Capturing less than 10% of the global semiconductor market while consuming 20% means Europe is a net importer on a massive scale and places its industrial base at the mercy of foreign suppliers. It also masks a far more critical vulnerability. The <10% of global production that Europe does possess is overwhelmingly concentrated in the mature-node semiconductors vital for its automotive and industrial champions. However, in the leading-edge logic nodes (sub-7nm) that power artificial intelligence, high-performance computing, and modern defense systems, Europe's production capacity is functionally zero. This is the true nature of the continent's structural deficit: it is not just a volume problem but rather a high-end technology void that directly translates into profound geopolitical and military vulnerability.

The European Chips Act of 2023 was a necessary response, but its ambition to reach 20% market share by 2030 is already failing. The European Court of Auditors (ECA) special report, published in 2025, provides the definitive "reality check." The ECA concluded that the 20% target, which would require quadrupling EU production, is "overly ambitious" and "deeply disconnected from reality". This objective, independent assessment creates the political and strategic necessity to abandon the failing "catch-up" strategy and pivot to a "Chips Act 2.0."

III. The Shifting Battlefield: Megatrends Demand An Asymmetric Strategy

The EU's current strategy is failing not only because its execution is flawed, but because it is fighting the last war. It aims to replicate an Asian-centric, commodity-manufacturing model at the very moment three new megatrends are rendering that model obsolete. These trends create a unique, fleeting opportunity for Europe to leapfrog the competition rather than futilely chase it.

Megatrend 1: The End of Monolithic Scaling (The "Moore's Law" Wall)

For half a century, chip performance came from one lever: shrink the transistor and ride the learning curve. That lever is failing. Many industry specialists argue that traditional scaling is encountering increasingly severe physical and economic constraints, even if incremental improvements remain possible. At the angstrom scale, managing electrical current becomes incredibly difficult as quantum tunneling and leakage become major constraints. While transistor innovations like FinFETs, gate-all-around (GAA) nanosheets, and forksheets help mitigate these issues, they significantly increase manufacturing complexity and cost.

Furthermore, thermal management now dictates chip architecture. Transistor density has outpaced our ability to cool the silicon, meaning modern chips feature ""dark silicon""—areas that must remain powered down to prevent overheating. To keep improving performance within these thermal envelopes, designers are forced to abandon simple scaling in favor of complex workarounds, such as domain-specific accelerators and aggressive power management, effectively ending the simple scale-and-win dynamic that defined the last era.

The economic wall is harsher. Each node turn now demands a step-change in EUV layers, mask counts, device options, and verification complexity. Development budgets jump by hundreds of millions, and only a handful of products can amortize that spend. Wafer costs and time-to-yield stretch program risk profiles, while the performance-per-watt delta between adjacent nodes narrows enough that system architects, meaning the firms and research organizations that design heterogeneous systems composed of multiple specialized chiplets integrated through advanced packaging often prefer architectural and packaging gains over a risky node migration. The classical ROI calculus that funded Moore's Law is broken for all but a tiny apex of products.

The consequence is a migration of value from monolithic die to heterogenous integration. Instead of one giant chip doing everything, performance will come from tightly integrated ensembles of specialized chiplets: dense logic on the best-fit node, high-speed I/O on a cost-effective node, stacked memory where bandwidth per watt matters more than raw density, and dedicated accelerators for data movement, security, compression, or signal processing. The package becomes the computer. Signal integrity, thermal design, power delivery networks, and die-to-die fabrics now govern the system budget as much as transistor density. That is why advanced packaging technologies are rapidly moving to the center of semiconductor innovation. Other major semiconductor regions including the United States, Japan, and South Korea have also launched initiatives to expand advanced packaging capabilities, recognizing its importance in future chip architectures such as 2.5D bridges and interposers, 3D hybrid bonding, backside power delivery, fine-pitch copper-to-copper interconnect, and standardized die interfaces, have turned from being afterthoughts into the new frontier of semiconductors.

This shift is a strategic reset of the entire industry. The geography of advantage moves from a handful of leading-edge fabs to a broader ecosystem of integrators, toolmakers, substrate innovators, test and reliability specialists, and standards bodies.

In this world, the decisive actors are the "system architects, meaning the firms and research organizations that design heterogeneous systems composed of multiple specialized chiplets integrated through advanced packaging" who can compose heterogeneous tiles into reliable, thermally sound, energy-efficient systems under real supply constraints.

Europe is unusually well positioned for this turn: it hosts the research nodes that define the packaging roadmap, the equipment champions that make fine-pitch and hybrid bonding possible, and the vertical markets such as automotive, industrial control, energy infrastructure, that already prize reliability, longevity, and safety certifications over bleeding-edge density. In short, when performance no longer comes "for free" from smaller transistors, the premium shifts to integration know-how and platform orchestration. That is a contest Europe can choose to lead.

Megatrend 2: China's "Commodity Trap" and the Fatal TCO Gap

Europe's attempt to rebuild broad-based commodity fabrication runs straight into an unforgiving cost reality. Fabs consume energy, water, land, equipment, and specialized labor at 24/7 scale; marginal disadvantages in each category compound into a structural total-cost gap that even generous subsidies struggle to neutralize over the lifetime of an asset. Electricity prices set the floor for every kilowatt-hour pushed through chillers, vacuum pumps, abatement systems, and tool stacks; water pricing and recycling targets dictate the economics of ultrapure-water plants and reclaim systems; permitting timelines lock in carrying costs and delay learning curves; and wage structures shape both direct labor and the cost of the deep maintenance crews that keep a modern line upright. Even where individual member states deliver preferential tariffs or fast-track approvals, the average European cost stack remains meaningfully above the best Asian and U.S. comparables, and those deltas widen precisely in downcycles when price pressure is fiercest.

Beijing is exploiting that gap with a volume-driven strategy that quietly corners the market. Instead of chasing the sanction-exposed, capital-intensive frontier, China is saturating the world with subsidized capacity at mature nodes—exactly the geometries that feed autos, industrial controls, power management, connectivity, and the long tail of IoT. The tactic is twofold. First, guarantee domestic sufficiency across a sprawling manufacturing base so that local OEMs never stall for lack of microcontrollers, PMICs, or basic connectivity ICs. Second, export the surplus to set global reference prices, compressing margins for every rival who pays more for power, water, labor, and debt. The playbook is familiar from solar and batteries: push enough scale through the fixed-cost stack that your unit economics look irresistible and your competitors' balance sheets look untenable.

For Europe, the trap is subtle because it looks like a jobs program in the short run. A mature-node fab tied to automotive demand appears to de-risk supply chains and anchor regional ecosystems. But as subsidized Chinese wafers clear the market at prices European plants cannot match through the cycle, the long-run business case erodes. Public money ends up defending the wrong cost curve. Worse, by concentrating on the same commodity geometries that Beijing has targeted, Europe reproduces the exact dependency structure it says it wants to escape: critical domestic industries become price-takers on parts of the stack where Europe's structural TCO is weakest.

The way out is to refuse the frame. If the total-cost game is unwinnable at scale, Europe must concentrate resources where TCO is not the dominant variable and where capability, integration, and certification erect barriers that subsidies cannot cheaply cross.

That means steering capital away from generic wafer acreage and into assets that compound: advanced packaging lines with fine-pitch hybrid bonding; qualification and security labs that make European chiplets the default for safety-critical domains; wide-bandgap materials and modules where device physics, reliability curves, and automotive grade standards matter more than cents per die; photonic interconnect and co-packaged optics where energy per bit becomes the contractual KPI; and the equipment houses whose tools every region needs regardless of geopolitics. It also means using demand power—EuroHPC JU, public clouds, mobility fleets, grid upgrades—to specify energy, latency, reliability, and lifecycle metrics that privilege European strengths. Rather than subsidize a forever price war on commodity wafers, Europe should fund

a portfolio that prices in system performance, safety, and sovereignty. In that portfolio, Chinese dumping pressures margins on some inputs, but cannot easily copy the integrated offering that Europe brings to market.

Megatrend 3: The "Leap-Frog" Playbook (China's EV, Semiconductor & AI Strategy)

When a nation is decades behind in a mature, capital-intensive, and path-dependent technology, it is strategic malpractice to attempt a "brute force" catch-up. Incumbents sit on mature IP, refined & complex supply chains, and learning-curve advantages that compound with every cycle. The winning move is to redefine the battlefield by identifying the next paradigm, concentrating on the new chokepoints, and render incumbents' legacy advantages less relevant. That is the essence of China's 21st century industrial strategy, first in electric vehicles and now in semiconductors and AI, and it's the playbook Europe should adapt to semiconductors.

In autos, China never tried to out-engineer Germany and Japan on the internal-combustion engine. It effectively "sat out" the ICE race and placed a three-decade bet on electrification. The country built the infrastructure and standards around batteries, supply of processed minerals, and high-efficiency motor manufacturing. The result was command of the value stack that actually determines EV cost curves—cell chemistry and manufacturing, mineral refining and active-material production, and rare-earth magnet supply for permanent-magnet motors. By the time Western OEMs pivoted in earnest, China's upstream and midstream capacity—from anode/cathode materials through cell lines to drive-unit components—was already scaled, integrated, and price-setting. Beijing didn't win by making a better V8; it made the V8 strategically irrelevant and then owned the components that make an EV cheap, reliable, and exportable.

China is applying the same move in semiconductors: rather than chase the most sanction-exposed, capital-hungry leading-edge nodes head-on, it is building durable moats where the next system bottlenecks are forming. That means flooding the world's demand in mature nodes that power autos/industrial/IoT; scaling memory where domestic architectures (e.g., novel NAND bonding schemes) can offset lithography gaps; pushing hard into advanced packaging and heterogeneous integration so multiple good-enough dies can outperform a single monolith; deepening local tool and materials supply in the steps least dependent on extreme EUV (etch, deposition, cleans, CMP, photoresists); and cultivating open architectures (notably RISC-V) plus chiplet-friendly design flows to reduce dependence on any one foundry or ISA. The net effect mirrors EVs: make the "frontier node" less of a chokepoint by shifting advantage to the layers you can control—volume at mature nodes, memory, packaging, power devices, and open IP—so that system-level cost and time-to-market tilt in your favor even if you never match the incumbent's absolute transistor density.

AI is replaying the same logic under different constraints. U.S. export controls and datacenter-class GPU restrictions created a hard compute gap. Rather than chase bigger models with scarcer accelerators, leading Chinese labs redirected effort toward algorithmic and systems efficiency: mixture-of-experts routing to reduce active parameters, compression and quantization to cut memory and bandwidth, curriculum and data deduplication to raise the quality of every training token, and inference-time optimization to squeeze latency and watts per query. Models like Qwen, DeepSeek, and Kimi illustrate the pattern: capability converging through efficiency rather than brute FLOPs. In other words, when the incumbent controls the obvious lever (compute), the challenger competes on the less obvious ones (architecture, data, systems engineering).

Europe now stands where China stood in the 1980s: crucial to the global industry but disadvantaged in the legacy paradigm. Even with the EU Chips Act, Europe will not out-TSMC TSMC or out-Samsung Samsung at the 2–3 nm frontier. The scale economics, yield learning, and capital cadence of leading-edge logic are structurally stacked against a new regional champion. And even where new European fabs are essential—for automotive, industrial, and secure supply at mature nodes—they are not the lever that will set the next thirty years of compute economics.

The leap-frog for Europe lies in the "post-Moore" bottlenecks—where system integration, materials, and packaging now determine performance per watt, time-to-market, and total cost. Advanced packaging is the first pillar. As scaling slows, value migrates from monolithic front-end to heterogeneous assembly: 2.5D interposers, 3D stacking, hybrid bonding, backside power delivery, and standardized die-to-die fabrics. Winning here means turning packaging into Europe's de facto new "front end," with

interoperable chiplet ecosystems that dilute single-foundry lock-in. The ingredients already exist: world-class bonding and die-attach tool makers; research depth at imec, CEA-Leti, and Fraunhofer; and anchor projects that can turn pilots into pan-European OSAT-grade capacity.

Europe should institutionalize a UCIe-centric compliance and security regime, tie public procurement (especially JU) to chiplet-based designs assembled in Europe, and finance at least two continental packaging houses capable of high-volume hybrid-bonded assemblies by the end of the decade. The outcome isn't just sovereignty; it's leverage—if everyone's compute becomes a multi-die system, the region that certifies, assembles, and qualifies those systems acquires structural pricing power.

Compound semiconductors are the second pillar. SiC and GaN are no longer niche: they are the efficiency engine for EV inverters and chargers, renewable integration, industrial drives, and the power-delivery networks of AI datacenters. Here Europe starts from strength. European champions already lead in SiC devices and modules, and the substrate and epitaxy base is scaling. Consolidating this lead—permitting, grid access, skilled-operator pipelines, and targeted state aid—yields a full "mine-to-module" chain inside the single market. If public fleets, charging networks, and grid-scale converters are specified to prefer European SiC/GaN modules where performance and cost justify it, demand certainty will accelerate learning curves and lock in exportable module designs.

The third pillar is optical I/O and co-packaged optics. AI clusters are increasingly bound by interconnect, not peak TOPS. Moving optical engines onto or into the package slashes power per bit and lifts bandwidth density, enabling cluster growth without linear energy penalties. Europe has the substrate technology, photonics research base, and packaging know-how to turn this into an industrial wedge: a CPO pilot-to-production pipeline linked to chiplet standards would let European integrators sell energy-efficient "Euro-packages" into global AI buildouts even when the compute tiles themselves are fabbed elsewhere. If EuroHPC JU and national clouds specify energy-per-bit and rack-level efficiency metrics that only CPO-class systems can meet, they will catalyze a home market large enough to matter.

There is also a quiet but decisive fourth pillar: equipment. ASML, ASM International, BESI, Zeiss, and a broader constellation of specialty toolmakers constitute Europe's deepest moat. Policies that expand their capacity, accelerate module innovation (ALD, hybrid bonding, backside vias), and train the next generation of process engineers compound that moat.

Equipment is leverage because every node, every package, and every region needs the tools; scaling European toolmakers therefore multiplies influence across supply chains Europe does not directly control.

What would success look like by the early 2030s? A European packaging complex that handles a meaningful share of global 2.5D/3D assemblies; a vibrant chiplet marketplace where European CPUs, accelerators, power-management dies, RF front-ends, security enclaves, and photonic I/O tiles interoperate under EU-certified standards; SiC and GaN modules that become default choices for EVs, charging, and grid retrofits; and AI systems deployed in EuroHPC JU that win on energy-efficiency and latency, not just on raw FLOPs. That configuration mirrors the EV and AI lessons: pick the chokepoints the incumbent underweights, master them end-to-end, and let the market's physics do the rest.

The temptation to recreate a leading-edge logic champion is understandable. But it is the industrial equivalent of building a better V8 in 1990—heroic, expensive, and misaligned with where advantage is migrating. A European leap-frog strategy recognizes that tomorrow's compute is assembled more than it is etched, powered by wide-bandgap materials more than by Dennard scaling, and connected optically more than electrically. Own those intersections and Europe stops playing catch-up; it starts setting the rules.

IV. Europe's Starting Position

A successful national strategy is not built on ambition alone; it must be rooted in an unvarnished assessment of a nation's underlying advantages and disadvantages. The current EU strategy fails to do this. A clear-eyed view reveals an asymmetric foundation: a critical weakness in one area (fabrication), fragmentation in another (capital/labor), but world-ending dominance in a third (upstream suppliers).

A. Strategic Endowments: Inputs, labs, financing, and production-ready talent

National competitive advantage in not inherited; it is manufactured through decades of deliberate investment. Europe's factor conditions are powerful where knowledge is the currency and fragile where commodity inputs dominate the cost stack. The profile is uneven and that unevenness should dictate strategy.

Europe's strongest endowment is its publicly anchored R&D infrastructure. Imec in Belgium, the Fraunhofer-Gesellschaft in Germany, and CEA-Leti in France have been defining the roadmaps of nanoelectronics and packaging for years. These institutes routinely demonstrate the "next step" first – hybrid bonding densities, backside power delivery, advanced interposers, co-packaged optics, and they do so with a consortium model that already includes the world's leading toolmakers and device companies. Europe's persistent failure was never invention; it was industrialization at scale. The Chips for Europe Initiative explicitly tries to close that gap by funding pilot lines and shared platforms so ideas do not die in the technology-transfer valley. The policy logic here is sound. If the post-Moore frontier is integration, then the pilot line is the new wafer fab where yield learning, reliability, and qualification are earned before capital goes truly heavy.

Capital, by contrast, is fragmented. The headline "€43 billion" attached to the Chips Act was never a single pot. The directly EU-budgeted share is small—on the order of €3.3 billion—augmented by a Chips Fund mechanism and, above all, by national state-aid packages unlocked under the "first-of-a-kind" framework. In practice that means subsidy firepower tracks national balance sheets rather than European priorities. Richer member states can write larger cheques faster, poorer ones cannot, and the policy degenerates into a race to host capacity rather than a plan to build advantage. External analyses have been blunt on this point: the €43 billion figure blends EU-level money with national and private financing, obscuring how little fresh, centralized EU capital is actually available to steer the strategy. The result is predictable—projects that clear a national politics bar, not necessarily a European competitiveness bar.

Human capital is misdiagnosed, and that misdiagnosis leads to misallocation. It is true that Europe will need tens of thousands of additional engineers and technicians by 2030. But the binding constraint is not the supply of STEM degrees in the abstract; it is where Europe's best graduates choose to work and how quickly they become "fab-ready." On the first axis, the industry loses talent not primarily to other countries but to other sectors. Top graduates chase compensation, equity, and perceived excitement in software, AI startups, and finance. On the second axis, the skills pipeline is misaligned: too many programs produce researchers who require years of on-the-job training to run a high-mix, high-reliability line; too few produce process, equipment, test, and packaging specialists who can be productive in months. If Europe pours tens of billions into concrete without fixing this, it will either strand under-utilized assets or raid its own champions to staff new sites, hollowing out the very firms that anchor the ecosystem today. The right metric is not graduates minted; it is time-to-productivity in pilot and production environments and the share of top-quartile graduates choosing semiconductors over software and finance.

B. Home Demand: Buyers, what they purchase, and how they specify it

A strong, sophisticated, and demanding domestic customer base is a primary driver of innovation. Firms forged by this tough local demand become global competitors. Here, Europe's market is split in two.

Europe's most valuable demand condition sits in its backyard: the automotive and industrial complex. €2.4 trillion of manufacturing value added and employs ~30 million people. Inside that base, the automotive sector alone contributes ~€273 billion of GVA (1.8% of EU GDP) and over 13 million total jobs, with ~12 million vehicles produced annually—clustered around Germany and a high-intensity CEE belt where autos account for >10% of manufacturing jobs. Regulatory pressure on safety and emissions forces adoption of advanced power electronics, sensors, and controllers, and OEM purchasing preferences reward longevity and quality of supply. That combination creates a predictable, defensible market for European device leaders and for any integration plays that raise system efficiency or reliability. In that sense, automotive and industrial are less a vertical and more a domestic "test range" that hardens products before they go global.

The ESMC joint venture in Dresden is what good demand-pull looks like. TSMC leads operations, backed by strategic investments from Bosch, Infineon, and NXP; the process mix (28/22 nm planar and 16/12 nm FinFET) targets precisely the nodes that bottlenecked Europe in 2021–2022; and the capacity is sized and timed for automotive and industrial ramps later in the decade.

It binds supply to the customers who matter most and bakes learning into a European cluster that includes tools, materials, and OSAT-adjacent services. As of August 2024 the project had ground-breaking and EU-cleared state aid; public details target ~40,000 wafer starts per month at maturity. That is industrial policy doing what it should: securing a domestically strategic tier without pretending it is the global frontier.

The paradox appears at the leading edge. The political goal of hosting <5 nm logic was pursued via massive subsidies for "FOAK" sites, most prominently Intel's proposed Magdeburg megafab. Two problems undermined the bet. First, Europe does not currently have a deep pool of domestic fabless customers taping out at those nodes; the notional demand would have been imported from U.S. design houses with longstanding supplier relationships and complex ecosystem gravity. Second, the economics were brittle. Energy, water, permitting, and labor cost deltas are structural, not cyclical, and they compound exactly when downcycles hit. By mid-2025 the wager collapsed: Intel formally cancelled the Magdeburg project amid a broader retrenchment. The episode exposes the fallacy of equating geographic presence with strategic control. A foreign-owned apex fab in Europe creates construction jobs and headlines; it does not create a European leading-edge demand base or a European roadmap authority.

C. The Upstream Monopolies: Suppliers, tools and materials Europe controls

Europe's most durable bargaining power sits upstream. A small set of EU-based firms supply equipment, optics, engineered substrates, and consumables that every advanced manufacturing region must procure to operate. The density of capability in this tier is unusual by any industrial standard and gives the Union levers it has not systematically applied.

ASML anchors this position as the sole provider of EUV scanners used for sub-7 nm logic, and a primary supplier of advanced DUV platforms. Carl Zeiss SMT is the exclusive source of the projection optics that make those scanners viable, including the High-NA modules that determine the cadence of the next generation. ASM International leads in atomic layer deposition and key epitaxy steps that have become non-optional for modern transistor and interconnect stacks. BESI sets the pace in fine-pitch hybrid bonding and high-reliability die attach, which now sit at the heart of 2.5D/3D integration and chiplet assembly. Soitec provides scale in engineered substrates, from FD-SOI for low-power and RF to wafers tailored for photonics and wide-bandgap devices. Around these anchors sits a materials and gases cluster that shapes uptime and defectivity: Merck KGaA in photoresists and patterning chemistries, BASF in electronic chemicals, Air Liquide in specialty gases, and TRUMPF in high-power lasers used in EUV light sources.

This configuration matters for three reasons. First, it confers pacing power. Roadmaps for scanners, optics, bonding, ALD, and substrates effectively set what is feasible in both front-end scaling and "post-Moore" 3D integration. With targeted co-investment and coordinated export policy, Europe can influence timing, feature availability, and qualification priorities rather than merely react to them. Second, it creates leverage in crises. Service parts, upgrades, and field engineering are operational chokepoints in any disruption; prioritizing access through contractual clauses

can keep European and allied critical lines running when supply is tight. Third, it shapes standards. Control at the tool and material layers allows Europe to embed telemetry, verification, and security features that propagate into global norms for trusted manufacturing and packaging.

The moat is not uniform. Single-point dependencies exist in EUV optics and in certain bonding platforms with limited second-source depth. Sub-tiers remain fragile where non-EU vendors supply lasers, vacuum systems, precision ceramics, or chemical precursors. Workforce concentration compounds the risk, since field service, applications engineering, and precision manufacturing capabilities are clustered in a handful of sites and face escalating poaching pressure as more regions scale fabs and packaging lines. Policy alignment is another weakness: national export decisions affecting EU-wide assets have at times proceeded without a consistent Union framework, diluting Europe's ability to trade access for guarantees.

The policy response should be practical and measurable. Treat upstream champions as strategic infrastructure with EU-level screening, tailored protective instruments where appropriate, and dedicated counter-intelligence focused on process IP and service data. Co-fund defined roadmap steps with deliverables that matter for sovereignty: High-NA production and service capacity; hybrid-bonding pitch reduction and throughput; ALD modules for backside power delivery; engineered substrates for photonics and wide-bandgap devices. Tie public money to availability for EU programs and to demonstrable learning-curve gains. Harden the sub-tiers through a prioritized vendor map for lasers, optics coatings, specialty gases, photoresist precursors, vacuum and metrology subsystems; where exposure is extra-EU, use joint procurement, strategic buffers, or minority stakes to secure continuity. Make export alignment an EU-level competence that links any additional restrictions on European tools and optics to reciprocal, written guarantees of foundry access and crisis prioritization from allies. Finally, scale talent specific to this tier by funding train-to-deploy academies co-run by ASML, Zeiss, ASM, BESI, Soitec, and materials firms, with time-to-productivity measured in months for installation, service, applications, and precision manufacturing roles.

Governance should track outcomes rather than intentions. Capacity indicators should include EUV and High-NA scanner output, installed base and throughput of hybrid bonders, ALD chamber shipments, and annual volumes of engineered substrates. Resilience indicators should capture dual-sourcing rates for critical sub-components, buffer coverage for optics, lasers, resists, and gases, and mean time to repair for critical tools at EU sites under stress-test conditions. Access indicators should record how many defense, grid, EuroHPC JU, and automotive safety programs are covered by priority service and spares, and how many chiplet and packaging qualifications have been completed on European tool and material stacks. Economic indicators should follow global profit-pool share for EU upstream firms, R&D intensity, and the cadence of major product releases, alongside licensing throughput times at the EU level.

The strategic implication is straightforward: the center of gravity of the Chips Act should tilt toward the things only Europe can supply or certify. Funding more commodity wafer acreage where Europe is high-TCO and late to scale burns public money to buy share in a market designed to crush margin. Funding pilot lines, packaging integration, qualification labs, and the expansion of these upstream monopolies compounds moats the rest of the world cannot easily replicate or replace.

Table 1 shows the EU's true "chokepoint" champions:

Table 1: Europe's true "chokepoint" champions

Company	Domain	Global Market Share / Position	Strategic Implication
ASML (Netherlands)	EUV Lithography	100% Monopoly	No leading-edge (<7nm) chip on Earth can be made without this EU firm.
Carl Zeiss SMT (Germany)	EUV High-NA Optics	100% Monopoly (Sole Supplier to ASML)	The most complex optical systems ever made; a captive, indispensable enabler of ASML's monopoly.
ASM International (Netherlands)	Atomic Layer Deposition (ALD)	>55% Market Share	ALD is a critical, non-substitutable process for depositing angstrom-scale films for 3D transistors.
BESI (Netherlands)	Hybrid Bonding	Market Leader	The key enabling tool for next-gen 3D chiplet stacking (the "post-Moore" transition).

D. The "Co-opetition" Dilemma (Firm Strategy, Structure & Rivalry)

Intense, localized, domestic rivalry is the single greatest spur to innovation and productivity. It is this relentless, home-market competition that forces firms to innovate, to optimize, and to constantly move up the value chain. Firms forged in this crucible (e.g., Japan's 1980s auto industry, Silicon Valley's 2000s software industry) are the ones that ultimately dominate globally.

The EU's policy intervention in this determinant is, therefore, profoundly self-defeating. Instead of fostering competition, Pillar 2 and the IPCEI framework use state aid to manage and mute rivalry, priotiizing short-term supply chain stability over the long-term creation of globally competitive domestic champions. This strategic miscalculation manifests in two primary ways:

The "Co-opetition" Trap (ESMC). The European Semiconductor Manufacturing Company (ESMC) is the sharpest example of this co-opetition trap. The ESMC in Dresden is a €10 billion joint venture between TSMC and its primary European customers Bosch, Infineon, and NXP. On the surface, this is the Act's single greatest success: a "demand-pull" project that directly binds a stable supply of 28 12nm chips to the exact domestic customers who were crippled by the 2021 shortage. However, as an act of industrial policy, it is a defensive peace treaty where a war for innovation was needed. The JV brings direct domestic rivals (Infineon, NXP, Bosch) into a formal partnership. This act of "co-opetition" solves their shared capacity problem but simultaneously neutralizes the competitive pressure that would have driven one of them to innovate. It removes the incentive for a European firm to attempt the difficult, risky, but strategically vital task of developing its own competing 28nm-class process. Why would Infineon invest billions in a high-risk R&D venture if it had a guaranteed, state-subsidized, and contractually-bound supply from the world's best-in-class foundry? This JV freezes European firms as customers and locks in their dependency on TSMC's technology roadmap.

The second, perhaps even more flawed pillar is the use of multi-billion-euro subsidies to lure EU giants (Intel in Magdeburg; TSMC in Dresden) to build "First-of-a-Kind" (FOAK) fabs. This approach fundamentally confuses geographic presence with sovereign control.

Sovereignty is not geography. A fab owned by Intel (U.S.) or TSMC (Taiwan) is not a "European" asset in any strategic sense. The core IP, the roadmap, the R&D leadership, and, crucially, the profits remain in Santa Clara or Hsinchu. Europe is effectively paying tens of billions to become a high-tech manufacturing colony, a low margin satellite where critical decisions are made by foreign CEOs accountable to foreign shareholders. Additionally, the multi-billion subsidies that would go to foreign firms like Intel or TSMC will bankroll a talent war Europe's own firms cannot win. Flush with public cash, such a large foreign firm can outbid for 3,000+ of the most skilled engineers and technicians from companies like Infineon, STMIcro, Bosch, and the very R&D institutes (e.g., Fraunhofer) meant to be the EU's seedbed of innovation. The state is, therefore, subsidizing the hollowing out of its own domestic industry.

What is the net effect of this dual strategy? It's muting rivalry among domestic firms while subsidizing the entry of foreign giants, which blocks the emergence of a new European champion while weakening the existing ones and this guarantees strategic failure. It may secure capacity, but it does so at the expense of building domestic competitive advantage. It risks turning the EU's own champions (Infineon, NXP) into mere, permanent customers of subsidized foreign-owned fabs operating on their own soil, creating a new, more durable dependency, not the independence the Chips Act sought.

V. The Limits Of Chips Act 1.0

Chips Act 1.0 succeeded in one crucial aspect: it gave Europe crisis tools it lacked in 2021. It did not, however, equip the Union to command the chokepoints that now define semiconductor power.

> The European Court of Auditors' Special Report (April 2025) is explicit that the headline objective to reach 20% of world production by 2030 was set without commensurate means and is "very unlikely" to be achieved. The core reasons are fragmented capital, weak central steer, and a bias toward expensive "first-of-a-kind" (FOAK) prestige sites that do not rest on durable European demand. In short, the Act can purchase capacity, but not control.

The most material structural change wrought by the Act has been in crisis governance. Under the monitoring and crisis-response pillar, the Commission can now escalate to a formal crisis stage and impose priority-rated orders on designated facilities. That authority matters and it was missing when automakers were price-takers during the 2020-2022 crunch. Still, this is a downstream mechanism that becomes relevant only when the house is already on fire as it does not improve long-run competitiveness, alter total cost of ownership, or build an indigenous design-to-packaging stack. As a result, Europe has better emergency plumbing but no new water source.

Market outcomes since 2024 make the pattern unambiguous. The supply-push, headline projects untethered from home demand have been the first to fail under real business pressure. Intel formally abandoned its Magdeburg plan in mid-2025 as part of a broader footprint retrenchment, a high-profile confirmation that subsidized entry cannot overcome structural cost gaps and absent European leading-edge design demand. Similarly, the STMicroelectronics/GlobalFoundries joint FD-SOI fab for Crolles was suspended in early 2025 amid market softness and partner reprioritization. By contrast, projects anchored in European demand or positioned at emerging chokepoints continued to move forward. The ESMC venture in Dresden with TSMC and Bosch, Infineon, and NXP as equity customers, broke ground in August 2024 and targets roughly 40,000 300-mm wafers per month across 28/22-nm planar and 16/12-nm FinFET processes, precisely the nodes that bottlenecked autos and industrials. In parallel, Silicon Box's panel-level advanced-packaging facility in Novara has moved from proposal to execution. The project secured formal European Commission approval for €1.3 billion in state aid in December 2024, clearing the final regulatory hurdle for the €3.2 billion site. By early 2025, the venture had selected engineering partners Stantec and Drees & Sommer to drive construction, maintaining its schedule for a 2028 operational launch. This gives the EU a credible beachhead in the "post-Moore" bottleneck where value is migrating. These outcomes collectively validate what the auditors warned: supply-push prestige bets are brittle; demand-pull and strategic-niche investments are executable.

The economics behind those divergent outcomes are rather stubborn. Energy is the second-largest operating cost after depreciation for a modern fab and a growing share for advanced packaging lines. In 2024, average EU industrial electricity prices were roughly €0.199/kWh versus €0.075/kWh in the United States and €0.082/kWh in China; forward price expectations suggest Europe will remain structurally dear through this decade. Water is the second structural headwind. Asian fabs routinely achieve 80-85% water reuse, while European plants are typically far less efficient, pushing up both intake and treatment costs exactly where node complexity and packaging thermals increase process-water intensity. Subsidy envelopes can mask these deltas for a time but cannot erase them across the cycle. Unless projects are paired with site-specific energy hedges and Taiwan-grade water-reuse mandates, their competitiveness decays as soon as markets soften.

Governance and finance compound the cost problem. The "€43 billion" aura that surrounded Chips Act communications blended small EU-level instruments with national cheques and private capital; the ECA's point is that the genuinely steerable EU pot is modest and dispersed, so strategy devolves into a contest among member-state balance sheets rather than a singular European competitiveness plan. Even where state-aid contracts now embed crisis-priority clauses, a genuine improvement, the selection of projects has too often followed political salience rather than the logic of chokepoints, and the result has been an import of foreign rivalry without the creation of domestic leaders. A foreign-owned apex fab on EU soil secures capacity

during good times, but leaves roadmaps, IP and, crucially, bargaining power outside the EU.

Using a five-forces assessment, we examine how Chips Act 1.0 has altered Europe's semiconductor market structure. Doing so, it becomes clear why the instrument mix underperforms. Entry looks deceptively high because FOAK subsidies reduce capital barriers on paper, but when sponsors pivot, as Intel did in Germany, the "entry" evaporates. Rivalry is muddled by design: customer joint ventures, while stabilizing supply, mute domestic process rivalry and entrench dependence on external roadmaps. Buyer power has improved where it matters most, because demand-anchored ventures and the crisis toolbox give autos, industrials, and governments leverage they lacked four years ago. Supplier power is unchanged or strong and in Europe's case that's a good thing. The world's most irreplaceable upstream assets, EUV lithography optics, ALD, hybrid bonding platforms, engineered substrates, remain European and every region's fab build-out increases global demand for those tools and materials. The lesson for a 2.0 pivot is obvious: stop diluting the one quadrant where Europe already dominates and re-point public capital toward it.

What, then, should change in practice? First, targeting must move from acreage to chokepoints. Funding generic wafer capacity in high-TCO geographies is a losing proposition through the cycle; funding advanced packaging, qualification and security labs for chiplets, and expansions in upstream tools and engineered materials compounds moats that others cannot quickly replicate. Second, instruments must reward demand-pull. The ESMC structure (customer equity and binding off-take) should be the default for any aid above the billion-euro threshold, with enforceable crisis-priority clauses embedded ex-ante. Third, enablers must be made contractual rather than aspirational. The economics only work if sites lock in decade-long low-carbon PPAs that neutralize the EU power premium and commit to ≥80% water reuse by year three; both can be de-risked with EU-level guarantees and co-funded on-site UPW/reclaim plants. Fourth, the scorekeeping must drop the metric of "share of global output" and replace it with sovereignty indicators that a Cabinet can govern against: share of global shipments in EUV optics, ALD and hybrid bonders; the number of EU-assembled hybrid-bonded 2.5D/3D systems qualified for automotive, defense and cloud; the proportion of designated defense bills-of-materials with priority-rated domestic supply paths demonstrated in quarterly stress tests; and site-level €/kWh and water-reuse performance versus published thresholds. As those indicators move, Europe's position moves in ways that cannot be unwound by a single corporate press release.

Eligibility Tests for Public Money

Does the project carry EU off-take from automotive, industrial, defense or cloud buyers that covers at least 60% of nameplate capacity for five years or more? If not, it fails the demand-anchor test.

Does it expand European control over equipment, materials, advanced packaging, or qualification/certification layers where replication is hard? If not, it fails the chokepoint test.

Are priority-rated order clauses embedded ex-ante with verification triggers and penalties for non-performance under crisis activation? If not, it fails the governance test.

With site-specific PPAs and water-reuse CAPEX, does modeled OPEX land within ±10% of a U.S. peer through the cycle? If not, it fails the TCO test.

Will staffing cannibalize EU champions or RTOs by more than 15% of critical teams? If yes, it must fund train-to-hire academies before groundbreaking.

Europe now has the proof points to pivot. Intel's Magdeburg cancellation and the Crolles suspension demonstrate the limits of buying volume share. ESMC and Silicon Box, by contrast, show how demand-pull and post-Moore chokepoints translate into executable projects that strengthen bargaining power.

> Chips Act 2.0 should therefore stop trying to win a commodity race that Europe is structurally priced out of, and start compounding the assets that already make Europe indispensable to everyone else's semiconductor ambitions.

The European Chips Act is a massive government intervention designed to deliberately reshape the industry's structure. However, its flawed premises have led to a strategy that is empirically failing, as confirmed by both independent auditors and the market itself.

A. An Industry Structure in Flux: The Act's Strategic Impact

Analyzing the Act's impact on the industry's competitive structure reveals its deep, internal contradictions.

Threat of New Entrants (Artificially High): Prior to the Act, the threat of new entrants in advanced fabrication was zero due to tens of billions in capital barriers. Pillar 2 is a policy tool designed to selectively erase this capital barrier for chosen entrants. By providing multi-billion euro subsidies, the government is paying the entry fee for giant, "first-of-a-kind" (FOAK) players like Intel and TSMC. This is a state-sponsored distortion, not a market-based entry.

Intensity of Rivalry (Artificially Muddled): The Act is strategically incoherent. It mutes domestic rivalry (the ESMC "co-opetition" model) while simultaneously importing foreign rivalry (subsidizing Intel and TSMC to compete with domestic champions). This strategically muddled approach risks weakening its own firms' capacity for innovation.

Bargaining Power of Buyers (Decreasing, by Design): This is the most explicit and likely-to-succeed goal of the Act. The 2021 shortage showed that EU automakers had zero bargaining power. The Act solves this through two mechanisms: (1) Increasing local supply by building the co-owned ESMC fab, and (2) Creating legal force via Pillar 3 (Crisis Response), which allows the Commission to impose "priority-rated orders" on fabs during a crisis.

Bargaining Power of Suppliers (Unaffected / Strengthened): The Act does almost nothing to alter the power of upstream suppliers. In Europe's case, this is a positive feedback loop. The world's most critical supplier, ASML, is European. The Chips Act, by subsidizing the construction of new fabs (Intel, ESMC), functions as a massive indirect subsidy to ASML and the entire EU upstream cluster (Zeiss, BASF, Soitec). This policy, therefore, strengthens the most dominant and profitable part of the EU's ecosystem.

Threat of Substitute Products (Non-Existent): In the modern digital economy, the threat of a substitute for semiconductors is zero. This lack of substitutes is precisely why the industry is so strategic and has become a geopolitical weapon.

B. The Auditor's Reality Check & The Tale of Two Fabs

The contradictory nature of this "dual strategy" supports the damning assessment delivered by the European Court of Auditors (ECA) in its April 2025 report. The ECA provides a critical, objective reality check:

The 20% by 2030 target is "overly ambitious" and "deeply disconnected from reality".

The Act was rushed into legislation out of a "sense of urgency" without a proper impact assessment.

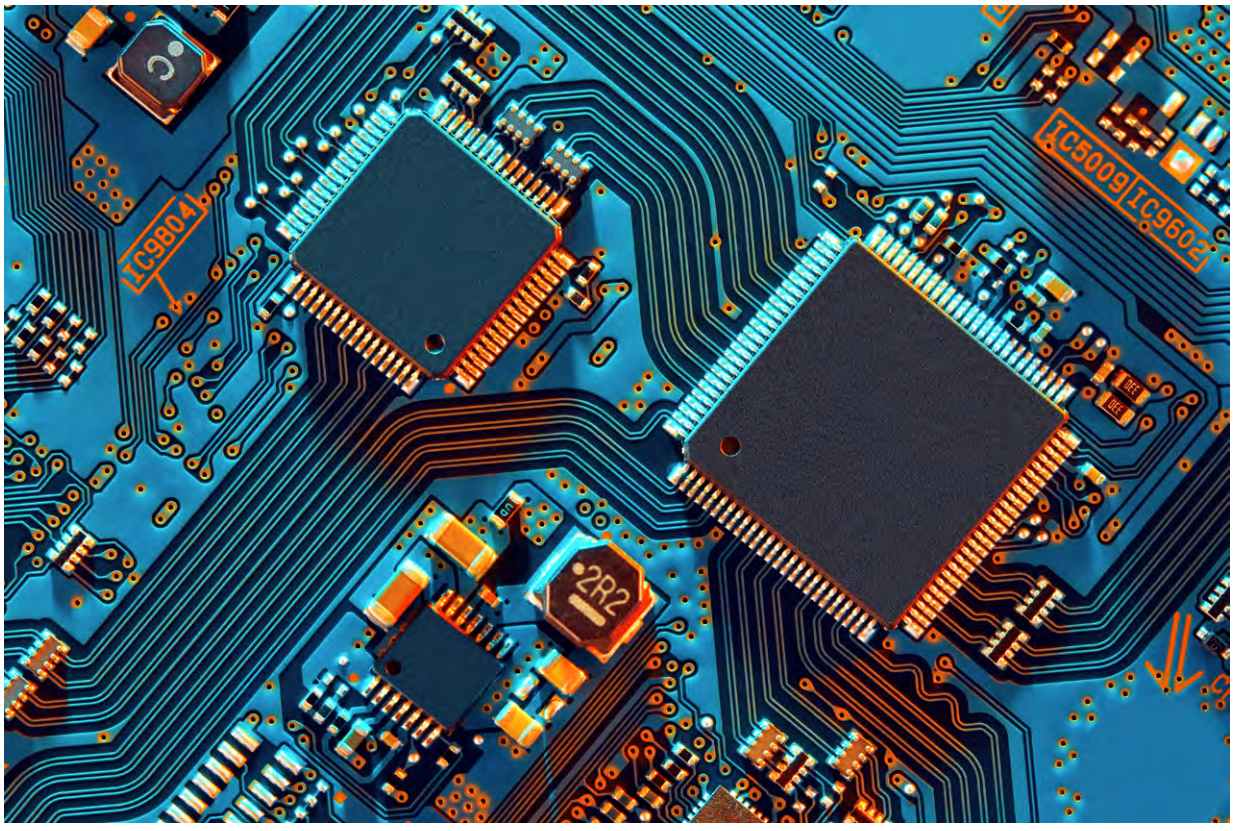
The EU's "financial muscle" is "fragmented and scattered" and dangerously reliant on a few large projects.

The market itself is providing an even more brutal, real-time verdict. The "dual strategy" of the Act has resulted in a clear, empirical split. The political, "supply-push" prestige projects are failing. The industrial, "demand-pull" and "strategic-niche" projects are succeeding.

The pattern becomes rather obvious. The "supply-push" projects (Intel, ST/GF) failed. The "demand-pull" (ESMC) and "strategic-niche" (Silicon Box) projects are succeeding. This provides the clear, evidence-based mandate for the strategic pivot this paper proposes.

Table 2: A Reality Check for Chips Act 1.0 (Status Q4 2025)

Project	Type	Technology	Demand Model	2025 Status (Q4)	Why it Matters
Intel (Magdeburg, DE)	Leading-Edge Logic	<2nm "Angstrom Era"	**Supply-Push:** "Build it and they will come." Lacks domestic EU demand.	**Cancelled:** Intel abandoned plans; German project ended	Confirms FOAK prestige bets are brittle without anchored EU demand and TCO parity.
ST/GF (Crolles, FR)	Niche Logic (FD-SOI)	<18nm	**Supply-Push:** Halted due to "weak market demand".	**Delayed but proceeding:** Partners suspended the €7.5B project in early 2025.	Illustrates demand fragility even at non-leading edge when economics tighten.
TSMC / ESMC (Dresden, DE)	Niche Logic (Auto)	28-12nm FinFET	**Demand-Pull:** JV with customers (Bosch, Infineon, NXP) ensuring guaranteed off-take.	**Proceeding:** Construction "well underway" as of June 2025.	Proves demand-anchored capacity tied to Europe's auto/industrial base is executable.
Silicon Box (Novara, IT)	Advanced Packaging	Chiplet Integration	**Strategic Niche:** Fills a known, high-growth "post-Moore" value chain gap.	**Proceeding:** €3.2B project approved. Construction starts 2H 2025	Builds the "post-Moore" choke-point Europe can own; anchors a packaging hub.
Infineon MEGAFAB-DD (DE)	Power/auto devices	Mixed nodes	**IDM, demand-linked**	**Approved;** €920M German aid (Feb 2025) with crisis-priority commitments	Strengthens Europe's industrial niches and formalizes crisis access.
Wolfspeed / Ensdorf (DE)	SiC power	SiC	**Supply-push**	**Cancelled:** (Oct 2025) amid demand softness	Wide-bandgap is strategic, but green-field commodity wafer acreage is exposed to cycles and TCO.



VI. Chips Act 2.0: A Plan For Indispensability

The failure of Chips Act 1.0, the calls from industry, and the formation of the "Semicon Coalition" by 9+ member states in March 2025 have created the political necessity for a "Chips Act 2.0". This new strategy must be asymmetric, disciplined, and built on the 10 pillars of European indispensability.

Pillar I: Secure and grow strategic core assets

Thesis: Europe's equipment and materials leaders (ASML, ASM, BESI, Zeiss, Soitec) are the EU's highest-leverage semiconductor capabilities. They underpin global leading-edge manufacturing and advanced packaging, give Europe agenda-setting influence over roadmaps and standards, and therefore must be protected, scaled, and used judiciously in economic statecraft.

Actions:

Protect: Designate the core IP, facilities, and service data of these firms as "Strategic European Infrastructure," with narrowly tailored EU-level tools: enhanced FDI screening, special share or veto rights limited to defined critical assets, and dedicated counter-intelligence and cyber programs to defend process IP and field-service telemetry. Harden sub-tiers (optics, lasers, specialty gases, precision ceramics) via supplier assurance, joint procurement, and continuity plans.

Fund: Co-invest on milestone-based terms in roadmap steps that lock in European pacing power: High-NA EUV production and service capacity; hybrid-bonding pitch reduction and throughput gains; ALD modules for backside power delivery; engineered substrates for photonics and wide-bandgap devices. Use repayable advances, matched private funding, and targeted tax credits. Expand train-to-deploy academies run with these firms to reduce time-to-productivity for installation, service, applications, and precision manufacturing roles.

Leverage (The "ASML Card"): Europe is failing to use its greatest weapon. The U.S. has unilaterally pressured the Netherlands to restrict ASML sales, imposing its foreign policy on an EU member state. Europe must move from a passive enforcer of U.S. policy to an active co-architect. All future EU-wide alignment with U.S. export controls (coordinated via Pillar X) must be transactional, demanding legally-binding reciprocal guarantees of U.S. foundry access for EU defense and critical industry.

Pillar II: Assure leading-edge access

Thesis: Europe needs leading-edge logic fabbing, but the "build it and they will come" subsidy model (Intel Magdeburg) is a proven failure. The new strategy must be based on the successful "ESMC model."

Actions:

Adopt the "ESMC Model": Mandate that all future state aid for new fabs is contingent on the "ESMC model". This means the project must be a joint venture with, or at minimum have binding, long-term off-take agreements from, European industrial and defense primes. This guarantees demand and prevents public funds from being wasted on "prestige projects."

Institutionalize Crisis Access: Formally embed "priority-rated order" clauses for defense and critical infrastructure (as defined by the ESSC in Pillar X) into the state aid agreements for every "Integrated Production Facility" (IPF) and "Open EU Foundry" (OEF). This grants the EU a legal right to "first-in-line" access during a supply crisis.

Pillar III: Own the strategic niche markets

Thesis: While chasing leading-edge logic, Europe has ignored its global dominance in the chips that run the entire green and industrial transition. This pillar makes that dominance a conscious, funded, and protected strategy.

Actions:

Compound the Lead in Wide-Bandgap: Go "all in" on next-generation Silicon Carbide (SiC) and Gallium Nitride (GaN). These compound semiconductors are the critical enablers of

electrification—essential for EV powertrains, 5G base stations, and advanced energy grids. Launch dedicated IPCEIs (Important Projects of Common European Interest) for this specific domain.

Support the Champions: Provide R&D and pilot line support for Europe's existing industrial champions—Infineon, NXP, STMicroelectronics, and Bosch—which are global leaders in automotive, industrial, and power chips.

Hardwire Demand: Use EU public procurement rules (for energy grids, rail, defense) and industrial standards to create a massive, stable "home market" for these high-performance European chips.

Pillar IV: Build advanced packaging hubs

Thesis: The end of Moore's Law (monolithic scaling) is the single greatest strategic opportunity for Europe. As the industry moves from single-die chips to multi-die "chiplets" (heterogeneous integration), the "back-end" packaging and assembly process becomes the new chokepoint. Europe missed the foundry wave; it can win the packaging wave.

Actions:

Build the Hubs: The €3.2 billion ($3.6B) Silicon Box investment in Novara, Italy, is the strategic beachhead. It brings first-of-its-kind, panel-level packaging to Europe. This project must be fully funded and fast-tracked as a European strategic priority, forming the anchor of a pan-European advanced packaging hub.

Connect the Ecosystem: Create 2–3 of these hubs that link R&D (IMEC, Fraunhofer), equipment (BESI's hybrid bonders), and high-volume manufacturing (Silicon Box).

Create Allied-Trusted Packaging: Establish EU–U.S.–Japan–Korea "trusted packaging" partnerships specifically for defense and AI systems. This makes Europe the secure "integrator" for allied defense systems, even if the chiplets are fabbed in the U.S. or Korea.

Pillar V: Make defense the anchor customer

Thesis: Treat chips as ammunition. The European Defence Agency (EDA) and NATO must become direct, funded partners in the EU's chip strategy, moving from being passive consumers to active, "first-in-line" customers.

Actions:

Fund "Trusted" Capacity: The demand signal is now explicit. The European Defence Fund (EDF) 2025 work program includes, for the first time, a topic for "Chiplet for Defence Application". This program seeks access to an "EU foundry" and a "common hardware library of chiplets" for military use. This demand must be met. Use EDF and national defense budgets to co-fund dedicated, secure, "trusted" production lines (e.g., radiation-hardened, long-lifecycle) within the new IPF/OEF fabs (Pillar II).

War Game the Supply Chain: Embed semiconductor supply chain scenarios (a Taiwan blockade, a cyber-attack on ASML, a repeat of the Nexperia crisis) into all major NATO and EU war games and exercises.

Strategic Stockpiling: Create a "strategic chip reserve" of critical, non-perishable defense and infrastructure components, managed by the EDA.

Pillar VI: Scale people and capability

Thesis: The "talent gap" is a misallocation and inefficiency crisis, not a simple shortage. Europe graduates ample engineers, but they are not "fab-ready" and are being lost to more "exciting" industries like AI and software.

Actions:

Fix the "Perception Gap": Launch a continental campaign to rebrand semiconductor manufacturing as a high-tech, high-impact field, essential for artificial intelligence and defense. This is necessary to compete with the cultural pull of AI and software startups.

Fix the "Inefficiency Gap": Fund "fab-ready" skills. Massively scale "train-to-hire" academies on-site at the new fabs, modeled on industry-academic partnerships. Public funds should subsidize talent conversion, not just construction.

Launch the "Semiconductor Erasmus": Supercharge the existing, small-scale Erasmus+ "METIS" program and the "European Chips Skills Academy" from €4 million pilot programs into a core, permanent pillar for cross-border talent mobility.

Anchor Political Legitimacy: Use chip investments for tangible regional regeneration (e.g., “Silicon Saxony” in Dresden, Novara in Italy). This creates high-tech, high-wage jobs and provides a political shield against narratives of corporate subsidies.

Pillar VII: Fix cost and infrastructure

Thesis: Europe’s high energy costs and slow permitting are a fatal TCO disadvantage that will kill any commodity fab. This must be reframed from a “green” liability into a “low-carbon TCO” weapon.

Actions:

Fix the “Boring” Stuff: Fabs are energy and water monsters. This strategy mandates one-stop, time-limited permitting and priority grid and water connections for all projects designated as IPCEI, IPF, or OEF.

Leverage Low-Carbon Energy as a TCO Weapon: The TCO of a fab in Asia is rising due to its reliance on volatile, coal-fired power. Europe can offer a superior long-term value proposition: long-term, price-stable energy contracts based on its low-carbon baseline (e.g., French nuclear, Nordic hydro). This stability is a competitive advantage to attract fabs and data centers that Asia cannot match.

Mandate Water Efficiency: Use the low recycling rates (10-14%) as a cudgel. All state aid must be contingent on recipients meeting “best-in-class” (i.e., Taiwanese ~80%) water recycling and reuse targets.

Pillar VIII: Mobilize EU-level capital

Thesis: The current “fragmented and scattered” model of national grants cannot compete in a $20 billion-per-fab world. Europe needs a dedicated, EU-level capital muscle.

Actions:

Establish the European Semiconductor Facility (ESF): Consolidate the patchwork of EIB/EIF initiatives and member-state funds into a single, empowered entity.

Mandate: The ESF’s mandate must be strategic, not just financial. It will be the primary financial tool of the European Semiconductor Security Council (Pillar X). It must have the flexibility to offer:

Long-term, low-interest loans (de-risking capex).

Equity co-investments (sharing upside, ensuring a strategic say).

Political risk insurance for strategic suppliers.

Pillar IX: Secure critical materials and inputs

Thesis: This entire strategy is useless if Europe swaps a dependency on Taiwanese fabs for a dependency on Chinese rare earths or Russian neon. The Nexperia and gallium/germanium crises of 2025 proved this.

Actions:

Map and Secure: Conduct an end-to-end “deep-tier” audit of the entire upstream value chain, from raw minerals (rare earths) to specialty chemicals and industrial gases (neon, palladium).

Diversify: Use the ESF (Pillar VIII) to fund joint procurement, strategic stockpiling, and co-investments in “friend-shored” (e.g., U.S., Canada, Australia) and domestic processing and recycling facilities.

Pillar X: Centralize governance and standards

Thesis: The current strategy is “fragmented” and failing because it lacks a central, empowered governing body.

Actions:

Establish the European Semiconductor Security Council (ESSC): The political opening is now. This strategy formalizes the “Semicon Coalition” of 9+ member states (launched in March 2025) and answers the industry-wide call for a “Chips Act 2.0”.

Mandate: The ESSC will be a permanent, high-level body with binding coordination powers. It will be the “conductor of the orchestra,” executing these 10 pillars and holding authority across funding (Pillar VIII), export controls (Pillar I), crisis response (Pillar 3 of the original Act), and allied diplomacy.

VII. Conclusion: From Exposure To Leverage

Sovereignty does not require owning every wafer, it requires being impossible to bypass. Since 2021 the EU has chased share of global output while industry power has shifted to equipment, materials, advanced packaging, and certification. Chips Act 2.0 should drop brute-force foundry replication and pursue indispensability: co-author export rules, tie any new fab subsidies to binding European off-take and crisis-priority rights, and measure success by leverage and access, meaning how many critical systems require a European tool, substrate, package, or certification to ship.

By 2035, the test is simple: can anyone field leading AI, electrified transport, secure industrial control, or defense systems without touching Europe? They should not. One continuously upgraded leading-edge access point in the EU, plus two or three packaging megasites that turn chiplets into qualified products, underpinned by European strength in SiC and GaN, engineered substrates, EUV optics, ALD, and hybrid bonding, should create a fabric of dependencies that no trade spat or single foundry decision can unwind.

Delivery needs institutions and cost realism. A European Semiconductor Security Council should coordinate funding, export controls, crisis allocation, and standards with binding authority. A European Semiconductor Facility should co-invest in tool, material, packaging, and security roadmaps and keep learning curves inside the single market, with long-tenor low-carbon power, Taiwan-grade water reuse, and site-level total-cost tests. Defense should act as first customer for trusted chiplet libraries and secure lines. EuroHPC JU, grid upgrades, and public fleets should specify energy per bit, latency, reliability, and lifecycle security to anchor a home market. Scale talent via on-site train-to-hire academies and a larger Semiconductor Erasmus.

A practical compact with allies: Europe guarantees access to its strategic core assets, including tools, materials, packaging, and secure integration, in exchange for treaty-grade access to leading-edge foundries and reciprocal crisis priority. With the right ecosystem, contracts, and institutions, Europe moves from price taker to rule setter in the post-Moore era. The credible end state is clear: nothing critical ships at scale without Europe.

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